MT6893 5G Smartphone Application Processor Technical Brief

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1 System Overview

The MT6893 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A/NR and C2K smart phone applications. The chip integrates four ARM® Cortex-A78 cores. One turbo core operates up to 3.0GHz and three operate 2.6 GHz, four ARM® Cortex-A55 cores operating up to 2.0 GHz and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and UFS/MMC/SD cards.

The application processor, an multi-core ARM® Cortex-A78, ARM® Cortex-A55 equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games.

All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

The high performance CPU, DSP, and hardware coprocessors are combined to provide a powerful modem subsystem capable of supporting NR Sub6, LTE Cat 18, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6893 also embodies wireless communication devices, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6893 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and media tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6893

- 1 ARM® Cortex-A78 cores operating at 3.0 GHz
- 3 ARM® Cortex-A78 cores operating at 2.6 GHz
- 4 ARM® Cortex-A55 cores operating at 2.0 GHz
- LPDDR4X up to 16 GB (four channels with 16-bit data bus width)
- Memory data rate up to LPDDR4X-4266
- LTE cat-18 4×4 MIMO
- NR Sub6 2CC with 200 MHz BW
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to QHD+ (1,440×3,360)
- OpenGL ES 3.2 3D graphic accelerator
- ISP supports 64MP@24 fps/192 MP capture
- AV1 4K@60 fps decoder
- HEVC 4K@60 fps decoder
- HEVC 4K@60 fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and wide-band AMR and EVS_WB)

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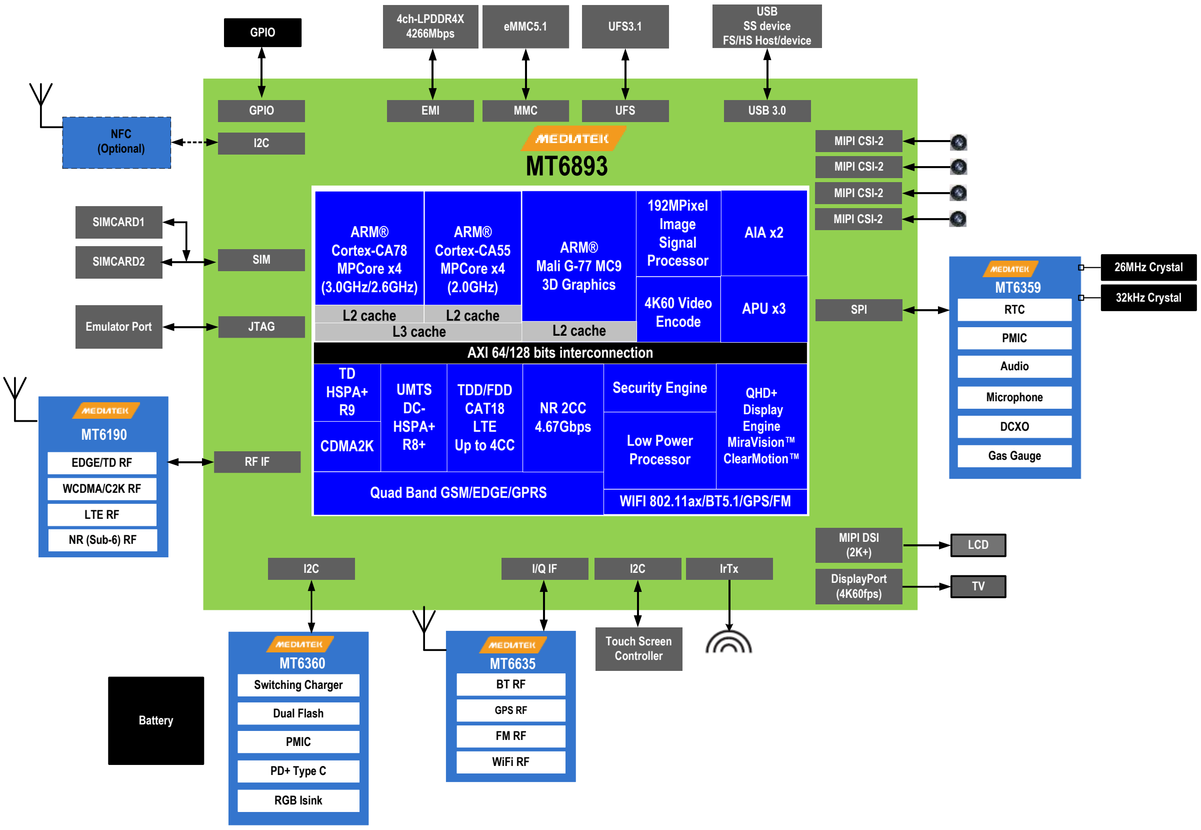

Figure 1-1. High-level MT6893 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, 2 MCU subsystems architecture
  - Supports eMMC/UFS boot
  - Supports LPDDR4X

- **AP MCU subsystem**
  - 4 ARM® Cortex-A78 cores with each core having 64 KB L1 I-cache, 64 KB L1 D-cache and 256 KB L2 cache. One turbo core operates up to 3.0GHz and three cores operate at 2.6GHz.
  - 4 ARM® 2.0 GHz Cortex-A55 cores with each core having 32 KB L1 I-cache, 32 KB L1 D-cache and 128 KB L2 cache
  - Shared 2 MB L3 cache
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - DVFS technology with adaptive operating voltage from 0.6V to 1.0V

- **Programmable Vision processor unit (VPU) to support both AI and CV**
  - Top performance: Fix8: up to 639 GMACs; Fix16: up to 160 GMACs; FP16: up to 80 GMACs, FP32: up to 40 GMACs
  - Dual core to support simultaneously multiple applications
  - vFPU to support high precision requirement applications

- **AI accelerator (AIA) (deep leaning accelerator: DLA) to support high computation demands NN applications**
  - Top performance: Fix8 1843 GMACs, Fix16 922 GMACs, FP16 461 GMACs
  - Simultaneous pipelined HW function block (CONV/ACT/POOL/EWE/BILINEAR)
  - Supports Android NN asymmetric quantized data format
  - Supports compressed weight to reduce DRAM BW

- **Memory subsystem in APUSYS**
  - 1 MB TCM as the 2nd level data memory
  - eDMA to reduce extra time for data transfer

- **MD MCU subsystem**
  - High-performance multi-core and multi-thread processor architecture
  - High-performance AXI bus interfaces
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR4X up to 16 GB (4 channels with 16-bit data bus width)
  - Memory data rate up to LPDDR4X-4266
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller’s I/O pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB one port with USB 3.0 device mode or USB2.0 OTG mode
  - eMMC5.1
  - UFS 3.1
  - 2 UARTs for debugging and applications
  - 8 SPI masters for external devices
  - 4 I2Cs/6 I3Cs to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module

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- Max. 4 PWM channels (depending on system configuration/IO usage)
- I2S for connection with optional external hi-end audio codec
- GPIOs
- 1 set of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO 2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.55~0.75V
  - I/O voltage: 1.8V/2.8V/3.15V
  - Memory: 0.75V
  - LCM interface: 1.8V
  - Clock source: 26 MHz, 32.768 kHz

- **Package**
  - Type: HBPOP
  - 12.4 mm × 12.4 mm
  - Height: Max. 0.64 mm (without DRAM on top)
  - Ball count: 977 balls
  - Ball pitch: 0.35 mm

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1.3 Modem Features

- **NR**
  - 3GPP EN-DC option 3/3a/3x
  - 3GPP SA option 2
  - FDD/TDD up to 4.67 Gbps downlink, 1.25 Gbps uplink
  - Supports downlink and uplink carrier aggregation (CA): 5~100 MHz RF bandwidth per component carrier (CC) and up to 2CCs with total 200 MHz BW
  - Supports SCS 15/30 kHz
  - Supports downlink/uplink 256 QAM
  - Supports downlink 4×4 MIMO and uplink 2×2 MIMO

- **LTE**
  - FDD/TDD up to 1.2 Gbps downlink, 150 Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4~20 MHz RF bandwidth per component carrier (CC) and up to 4 CCs
  - Uplink intra-band carrier aggregation (CA) ability; 1.4~20 MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - Supports downlink 256QAM/uplink 64QAM
  - 4×2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports MBMS
  - Uplink CoMP ability
  - Advanced interference cancellation
    - PDCCH pIRC
    - CRS-based PDSCH
    - DMRS-based Co-UE
  - Transmit antenna selection

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16 QAM), throughput up to 11.5 Mbps
  - Downlink Cat. 24 (64 QAM, dual-cell HSDPA), throughput up to 42.2 Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancement
  - Transmit antenna selection

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA bands 34, 39, 40 and quad-band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384 Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8 Mbps DL (Cat.14)
  - TD-HSUPA: 2.2 Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection
  - Transmit antenna selection

- **Radio interface and baseband front-end**
  - IQ data through high speed serial interface (DigRF) between RF and baseband chip
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) and MIPI RFFE interface with programmable driving strength
  - Supports multi-band

- **GSM modem and voice codec**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction

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- Digital side-tone generator with programmable gain
- 2 programmable acoustic compensation filters
- GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS GEA1, GEA2 and GEA3 ciphering
- Programmable GSM/GPRS/EDGE modem
- Packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GSM circuit switch data
- GPRS/EDGE Class 12
- Supports SAIC (single antenna interference cancellation) technology
- VAMOS (voice services over adaptive multi-user channels on one slot) technology in R9 spec
- Transmit antenna selection
- RF dual-antenna reception

- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6 kbps for forward and reverse links and DO data rates of 3.1 Mbps for forward link and 1.8 Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Supports simultaneous hybrid dual receiver (SHDR)
  - Supports 1x diversity
  - Supports SRLTE
  - Transmit antenna selection

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and wide-band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o wind noise rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.4 Connectivity Features

MT6893 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM receiver

The RF parts of those four blocks are placed on chip MT6635. With four advanced radio technologies integrated on one chip, MT6893/MT6635 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated radio coexistence algorithms and hardware mechanisms. It supports dual (MT6635) antenna sharing among 2.4 GHz Bluetooth, 2.4 GHz/5 GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and media tablets. The small footprint with low-power consumption greatly reduces PCB layout resource.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Dual antenna for WLAN
  - Single/Dual antenna for WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Dual-band (2.4/5 GHz) with 2 stream 802.11 ax/ac/a/b/g/n MAC/BB/RF SoC, 20/40/80 MHz bandwidth, MCS0~11 (1,024-QAM)
  - 802.11 d/e/h/i/j/k/r/v compliant
  - Security: WFA WPA/WPA2 personal, AES-CCMP, WPI-SMS4, GCMP, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS feedback, 20/40 MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports 802.11ax STBC Tx/Rx, 4T2R beamformee, 2T2R beamformer, MU-MIMO Rx, WoWLAN
  - Supports MediaTek proprietary low power green AP mode for portable hotspot operation
  - Auto rate control for optimizing the signal range and performance
  - Supports Wi-Fi direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated PA with 2.4G max. power 23 dBm for CCK; 5G max. power 19 dBm for 54 mbps OFDM
  - 2.4G Rx sensitivity is -76.5 dBm for 11n HT20 MCS7; 5G Rx sensitivity is -63 dBm for 11ac VHT80 MCS9
  - Supports 32 multicast address filters and TCP/UDP/IP checksum offload
  - Per packet Tx power control

- **Bluetooth**
  - Supports Bluetooth 5 dual mode for LE 2 Mbps, LE long range, and advertise extension
  - Supports BT 5.1 isochronous channels feature and following spec. certification
  - Integrated PA with 14 dBm (class 1) transmit power.
  - Rx sensitivity@chip-in:
    - GFSK -97 dBm
    - DQPSK -96 dBm
    - 8-DPSK -90 dBm
    - BLE_1M -100 dBm
    - BLE_2M -97 dBm

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    - BLE_500K -102 dBm (PER < 30.8%)
    - BLE_125K -106 dBm (PER < 30.8%)
  - Supports BT/Wi-Fi/LTE/NR coexistence
  - Supports 7 BT links and 16 BLE links
  - Supports packet loss concealment (PLC) function for better voice quality
  - Supports wideband speech
  - Supports mSBC and SBC including mono and stereo
  - Supports secure connection with AES128 and ECC256
  - Supports adaptive frequency hopping with built-in channel assessment method

- **GPS**
  - Supports L1 GPS/GLONASS/BeiDou/Galileo/QZSS concurrent reception
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
    - GPS/GLONASS/BeiDou (G+G+B)
    - GPS/Galileo/GLONASS (G+G+G)
    - GPS/Galileo/GLONASS/BeiDou (G+G+G+B)
  - Supports SBAS (satellite-based augmentation systems): WAAS/MSAS/EGNOS/GAGAN
  - Supports L5 GPS/Beidou-III B2A/Galileo-E5a/NavIC concurrent reception
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity
    - Coarse time assistance is 8 dB design margin over 3 GPP minimum requirement.
    - Fine time assistance is 10 dB design margin over 3 GPP minimum requirement.
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones for both L1 and L5 bands
  - Supports both TCXO and TMS (thermister crystal) clock source
  - 5 Hz update rate

- **FM**
  - 65~108 MHz with 50 kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2 dBµVemf (SINAD = 26 dB)
  - Audio SINAD 60 dB
  - Anti-jamming

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to QHD+ 21:9 (1,440×3,360), frame rate up to 90 Hz
  - Support 1,440×3,360@90 Hz panel and 1,080×2,520@144 Hz panel
  - DisplayPort 1.4
  - MIPI DSI interface (8 data lanes)
  - MiraVision™ for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 8 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Supports GPU decoder (AFBC)
  - Supports hardware wide-color-gamut (WCG)

- **Graphics**
  - 3D graphic accelerator capable of processing 30,096M pixel/sec@836 MHz
  - OpenGL ES 3.2/3.1/3.0/2.0/1.1
  - Vulkan 1.1/1.0
  - OpenCL 2.2

- **Image**
  - Integrated image signal processor supports 64 MP@30 fps preview/192 MP capture.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Multi-scale noise reduction for single frame/multi-frame image capture
  - Temporal noise reduction for video recording
  - Anti-blooming correction
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Deep learning face detection
  - Video face beautification
  - Zero shutter delay image capture
  - Supports high frame rate sensor (16 + 4M/120 fps)
  - Four MIPI CSI-2 high-speed camera serial interfaces; max. 4 data lanes of D-DHY; max. 3 trios of C-PHY
  - Supports maximum 3 trios of C-PHY 4.5 Gsps
  - Dual CAM, [32MP + 16MP]@30 fps
  - Tri CAM, [16 MP + 16 MP + 16 MP]@30 fps
  - Supports video HDR for stagger HDR sensor (16M30fps 3exp, 64X)
  - Supports video HDR for 4-cell HDR sensor (64 MP@30 fps 3exp, 64X)
  - Dual-stream video HDR
  - Dual PD/QPD HW accelerator
  - Throughput can afford SMVR HD960 sensor read out.
  - YUV frame buffer compression to reduce DRAM BW requirement
  - Hardware JPEG encoder: Baseline encoding with 800M pixel/sec.
  - Supports YUV422/YUV420 color format and EXIF/JFIF format
  - Baseline JPEG decoding throughput @YUV420, ≥ 64M pixels: 314M pixels/sec.
  - Dual cam real-time depth

- **Video**
  - HEVC decoder: 10-bit main profile, 4K2K@60 fps/160 Mbps

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- VP9 decoder: profile0 and profile2, 4K2K@60 fps/100 Mbps
- AV1 decoder: Main profile, 4K2K@60 fps/100 Mbps
- H.264 decoder: Baseline profile, 4K2K@60 fps/160 Mbps
- H.264 decoder: Main/High profile 4K2K@60 fps/160 Mbps
- Sorenson H.263/H.263 decoder: Baseline profile, 1,080p@60 fps/60 Mbps
- MPEG-4 SP/ASP decoder: Simple profile L6 and advanced simple profile L5, 1,080p@60 fps/60 Mbps
- DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1,080p@60 fps/60 Mbps
- MPEG2 decoder: Main profile, 1,080p@60 fps/60 Mbps
- VP8 decoder 1,080p@60 fps/40 Mbps
- HEIF decoder: 10-bit main profile, max. resolution 16,383×16,383
- MPEG-4 Software encoder: 720×480@30 fps, 4 Mbps. Simple profile level 6, advanced simple profile level 5
- H.263 software encoder: 640×480@30 fps, 4 Mbps. Profile 0 (baseline profile)
- H.264 hardware encoder: 10-bit high profile 4K2K@30 fps, 100 Mbps
- HEVC hardware encoder: 10-bit main profile 4K2K@60 fps, 160 Mbps

- **Audio**
  - Audio content sampling rates supported: 8~192 kHz (up to 384 kHz for I2S)
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, mono/stereo (up to 32-bit for I2S)
  - Interfaces supported: I2S, PCM
  - External codec I2S interface supports 16-bit/24-bit/32-bit, mono/stereo, 8~384 kHz.
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness (MB-DRC), BesSurround, Android built-in post processing
  - Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM
  - Voice wakeup

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

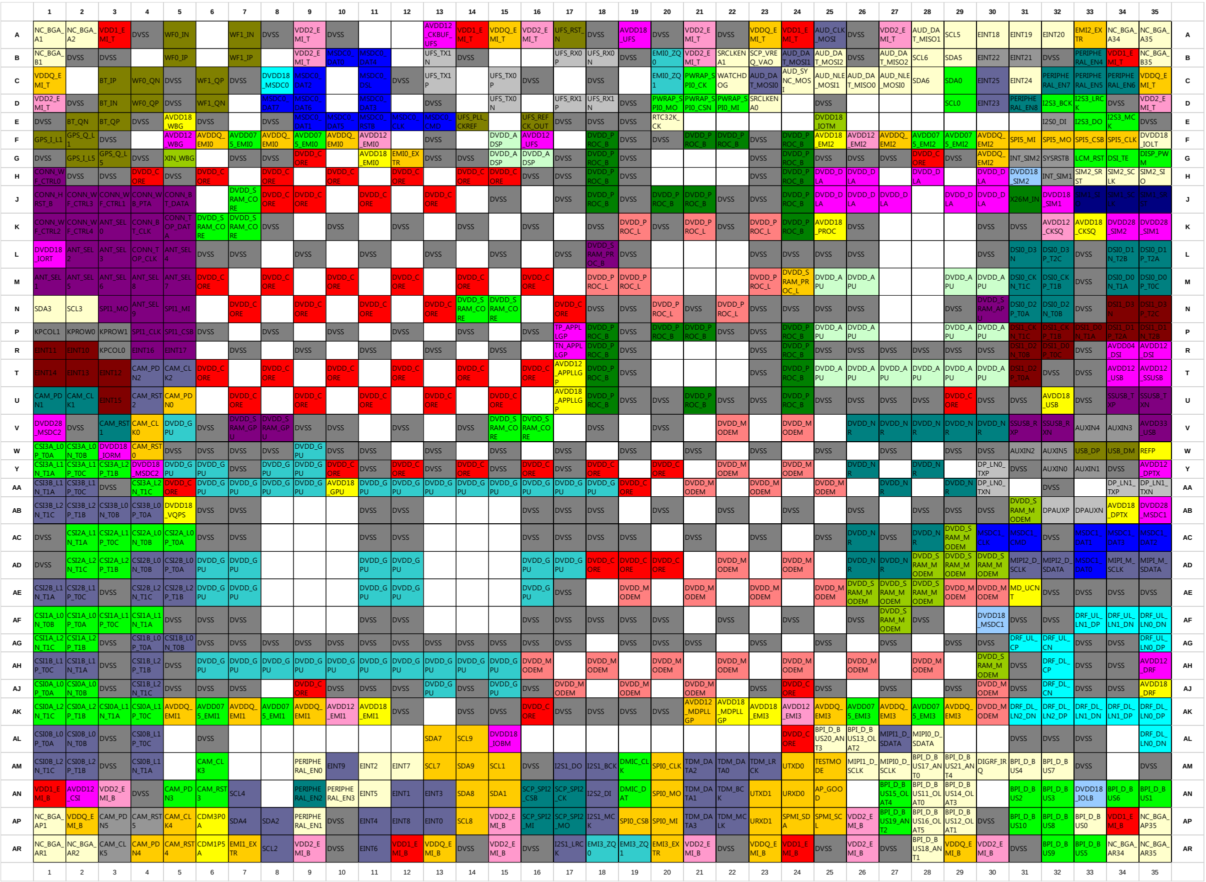

Figure 2-1. LPDDR4X ball map view

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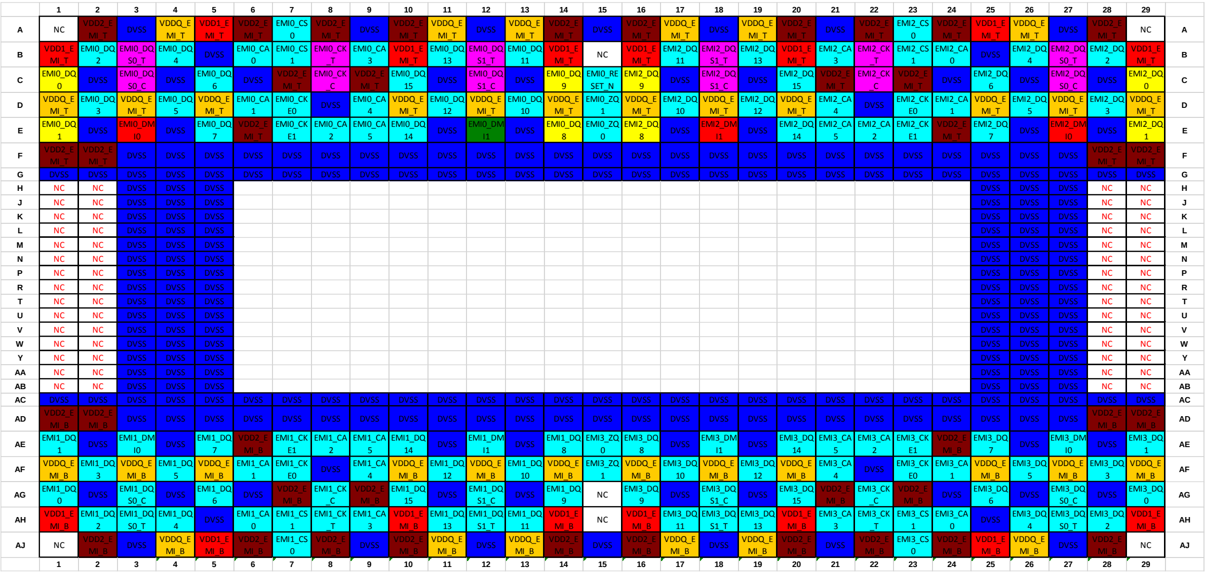

Figure 2-2. LPDDR4X TOP ball map view

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate LPDDR4X

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC_BGA_A1	AM13	SCL7	J17	DVSS
A10	DVSS	AM14	SDA9	J18	DVDD_PROC_B
A13	AVDD12_CKBUF_UFS	AM15	SCL1	J19	DVSS
A14	VDD1_EMI_T	AM16	DVSS	J2	CONN_WF_CTRL3
A15	VDDQ_EMI_T	AM17	I2S1_DO	J20	DVDD_PROC_B
A16	VDD2_EMI_T	AM18	I2S1_BCK	J21	DVDD_PROC_B
A17	UFS_RST_N	AM19	DMIC_CLK	J22	DVSS
A18	DVSS	AM2	CSI0B_L2P_T1B	J23	DVSS
A19	AVDD18_UFS	AM20	SPI0_CLK	J24	DVDD_PROC_B
A2	NC_BGA_A2	AM21	TDM_DATA2	J25	DVDD_DLA
A20	DVSS	AM22	TDM_DATA0	J26	DVDD_DLA
A21	VDD2_EMI_T	AM23	TDM_LRCK	J27	DVDD_DLA
A22	DVSS	AM24	UTXD0	J29	DVDD_DLA
A23	VDDQ_EMI_T	AM25	TESTMODE	J3	CONN_WF_CTRL1
A24	VDD1_EMI_T	AM26	MIPI1_D_SCLK	J30	DVDD_DLA
A25	AUD_CLK_MOSI	AM27	MIPI0_D_SCLK	J31	X26M_IN
A26	DVSS	AM28	BPI_D_BUS17_ANT0	J32	DVDD18_SIM1
A27	VDD2_EMI_T	AM29	BPI_D_BUS21_ANT4	J33	SIM1_SIO
A28	AUD_DAT_MISO1	AM3	DVSS	J34	SIM1_SCLK
A29	SCL5	AM30	DIGRF_IRQ	J35	SIM1_SRST
A3	VDD1_EMI_T	AM31	BPI_D_BUS4	J4	CONN_WB_PTA
A30	EINT18	AM32	BPI_D_BUS7	J5	CONN_BT_DATA

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A31	EINT19	AM33	DVSS	J7	DVDD_SRAM_CORE
A32	EINT20	AM35	DVSS	J8	DVDD_CORE
A33	EMI2_EXTR	AM4	CSI0B_L1N_T1A	J9	DVDD_CORE
A34	NC_BGA_A34	AM6	CAM_CLK3	K1	CONN_WF_CTRL2
A35	NC_BGA_A35	AM9	PERIPHERAL_EN0	K10	DVSS
A4	DVSS	AN1	VDD1_EMI_B	K12	DVSS
A5	WF0_IN	AN10	PERIPHERAL_EN3	K14	DVSS
A7	WF1_IN	AN11	EINT5	K16	DVSS
A8	DVSS	AN12	EINT1	K18	DVSS
A9	VDD2_EMI_T	AN13	EINT3	K19	DVDD_PROC_L
AA1	CSI3B_L1N_T1A	AN14	SDA8	K2	CONN_WF_CTRL4
AA10	AVDD18_GPU	AN15	SDA1	K20	DVSS
AA11	DVDD_GPU	AN16	SCP_SPI2_CSB	K21	DVDD_PROC_L
AA12	DVDD_GPU	AN17	SCP_SPI2_CK	K22	DVSS
AA13	DVDD_GPU	AN18	I2S2_DI	K23	DVDD_PROC_L
AA14	DVDD_GPU	AN19	DMIC_DAT	K24	DVDD_PROC_B
AA15	DVDD_GPU	AN2	AVDD12_CSI	K25	AVDD18_PROC
AA16	DVDD_GPU	AN20	SPI0_MO	K26	DVSS
AA17	DVDD_GPU	AN21	TDM_DATA1	K3	ANT_SEL0
AA18	DVDD_GPU	AN22	TDM_BCK	K30	DVSS
AA19	DVDD_CORE	AN23	UTXD1	K31	DVSS
AA2	CSI3B_L1P_T0C	AN24	URXD0	K32	AVDD12_CKSQ
AA21	DVDD_MODEM	AN25	AP_GOOD	K33	AVDD18_CKSQ
AA23	DVDD_MODEM	AN27	BPI_D_BUS15_OLAT4	K34	DVDD28_SIM2
AA25	DVDD_MODEM	AN28	BPI_D_BUS11_OLAT0	K35	DVDD28_SIM1
AA27	DVDD_NR	AN29	BPI_D_BUS14_OLAT3	K4	CONN_BT_CLK
AA29	DVDD_NR	AN3	VDD2_EMI_B	K5	CONN_TOP_DATA
AA3	DVSS	AN31	BPI_D_BUS2	K6	DVDD_SRAM_CORE
AA30	DP_LN0_TXN	AN32	BPI_D_BUS3	K7	DVDD_SRAM_CORE
AA32	DVSS	AN33	DVDD18_IOLB	K8	DVSS
AA34	DP_LN1_TXP	AN34	BPI_D_BUS6	L1	DVDD18_IORT
AA35	DP_LN1_TXN	AN35	BPI_D_BUS1	L11	DVSS
AA4	CSI3A_L2N_T1C	AN4	DVSS	L13	DVSS
AA5	DVDD_CORE	AN5	CAM_PDN3	L15	DVSS
AA6	DVDD_GPU	AN6	CAM_RST3	L17	DVSS
AA7	DVDD_GPU	AN7	SCL4	L18	DVDD_SRAM_PROC_B
AA8	DVDD_GPU	AN9	PERIPHERAL_EN2	L19	DVSS
AA9	DVDD_GPU	AP1	NC_BGA_AP1	L2	ANT_SEL2
AB1	CSI3B_L2N_T1C	AP10	DVSS	L23	DVSS
AB11	DVSS	AP11	EINT4	L24	DVSS
AB12	DVSS	AP12	EINT8	L25	DVSS
AB16	DVSS	AP13	EINT0	L26	DVSS
AB17	DVSS	AP14	SCL8	L3	ANT_SEL3

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AB18	DVSS	AP15	VDD2_EMI_B	L30	DVSS
AB2	CSI3B_L2P_T1B	AP16	SCP_SPI2_MI	L31	DSI0_D3N
AB20	DVSS	AP17	SCP_SPI2_MO	L32	DSI0_D3P_T2C
AB22	DVSS	AP18	I2S1_MCK	L33	DVSS
AB24	DVSS	AP19	SPI0_CSB	L34	DSI0_D1N_T2B
AB26	DVSS	AP2	VDDQ_EMI_B	L35	DSI0_D1P_T2A
AB28	DVSS	AP20	SPI0_MI	L4	CONN_TOP_CLK
AB29	DVSS	AP21	TDM_DATA3	L5	ANT_SEL4
AB3	CSI3B_L0N_T0B	AP22	TDM_MCLK	L6	DVSS
AB30	DVSS	AP23	URXD1	L7	DVSS
AB31	DVDD_SRAM_MODEM	AP24	SPMI_SDA	L9	DVSS
AB32	DPAUXP	AP25	SPMI_SCL	M1	ANT_SEL1
AB33	DPAUXN	AP26	VDD2_EMI_B	M10	DVDD_CORE
AB34	AVDD18_DPTX	AP27	BPI_D_BUS19_ANT2	M12	DVDD_CORE
AB35	DVDD28_MSDC1	AP28	BPI_D_BUS16_OLAT5	M14	DVDD_CORE
AB4	CSI3B_L0P_T0A	AP29	BPI_D_BUS12_OLAT1	M16	DVDD_CORE
AB5	DVDD18_VQPS	AP3	CAM_PDN5	M18	DVDD_PROC_L
AB6	DVSS	AP30	DVSS	M19	DVDD_PROC_L
AB7	DVSS	AP31	BPI_D_BUS10	M2	ANT_SEL5
AC1	DVSS	AP32	BPI_D_BUS8	M23	DVDD_PROC_L
AC11	DVSS	AP33	BPI_D_BUS0	M24	DVDD_SRAM_PROC_L
AC12	DVSS	AP34	VDD1_EMI_B	M25	DVDD_APU
AC16	DVSS	AP35	NC_BGA_AP35	M26	DVDD_APU
AC17	DVSS	AP4	CAM_RST5	M29	DVDD_APU
AC18	DVSS	AP5	CAM_CLK4	M3	ANT_SEL6
AC19	DVSS	AP6	CDM3P0A	M30	DVDD_APU
AC2	CSI2A_L1N_T1A	AP7	SDA4	M31	DSI0_CKN_T1C
AC21	DVSS	AP8	SDA2	M32	DSI0_CKP_T1B
AC23	DVSS	AP9	PERIPHERAL_EN1	M33	DVSS
AC25	DVSS	AR1	NC_BGA_AR1	M34	DSI0_D0N_T1A
AC26	DVDD_NR	AR10	DVSS	M35	DSI0_D0P_T0C
AC27	DVSS	AR11	EINT6	M4	ANT_SEL8
AC28	DVDD_NR	AR12	VDD1_EMI_B	M5	ANT_SEL7
AC29	DVDD_SRAM_MODEM	AR13	VDDQ_EMI_B	M6	DVDD_CORE
AC3	CSI2A_L1P_T0C	AR14	DVSS	M8	DVDD_CORE
AC30	MSDC1_CLK	AR15	VDD2_EMI_B	N1	SDA3
AC31	MSDC1_CMD	AR16	DVSS	N11	DVDD_CORE
AC32	DVSS	AR17	I2S1_LRCK	N13	DVDD_CORE
AC33	MSDC1_DAT1	AR18	EMI3_ZQ0	N14	DVDD_SRAM_CORE
AC34	MSDC1_DAT3	AR19	EMI3_ZQ1	N15	DVDD_SRAM_CORE
AC35	MSDC1_DAT2	AR2	NC_BGA_AR2	N17	DVDD_CORE
AC4	CSI2A_L0N_T0B	AR20	EMI3_EXTR	N18	DVSS
AC5	CSI2A_L0P_T0A	AR21	VDD2_EMI_B	N19	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AC6	DVSS	AR22	DVSS	N2	SCL3
AC7	DVSS	AR23	VDDQ_EMI_B	N20	DVDD_PROC_L
AD1	DVSS	AR24	VDD1_EMI_B	N21	DVSS
AD11	DVDD_GPU	AR25	DVSS	N22	DVDD_PROC_L
AD12	DVDD_GPU	AR26	VDD2_EMI_B	N23	DVSS
AD16	DVDD_GPU	AR27	DVSS	N24	DVSS
AD17	DVDD_GPU	AR28	BPI_D_BUS18_ANT1	N25	DVSS
AD18	DVDD_CORE	AR29	VDDQ_EMI_B	N26	DVSS
AD19	DVDD_CORE	AR3	CAM_CLK5	N29	DVSS
AD2	CSI2A_L2N_T1C	AR30	VDD2_EMI_B	N3	SPI1_MO
AD20	DVDD_CORE	AR31	DVSS	N30	DVDD_SRAM_APU
AD22	DVDD_MODEM	AR32	BPI_D_BUS9	N31	DSI0_D2P_T0A
AD24	DVDD_MODEM	AR33	BPI_D_BUS5	N32	DSI0_D2N_T0B
AD26	DVDD_NR	AR34	NC_BGA_AR34	N33	DVSS
AD27	DVDD_NR	AR35	NC_BGA_AR35	N34	DSI1_D3N
AD28	DVDD_SRAM_MODEM	AR4	CAM_PDN4	N35	DSI1_D3P_T2C
AD29	DVDD_SRAM_MODEM	AR5	CAM_RST4	N4	ANT_SEL9
AD3	CSI2A_L2P_T1B	AR6	CDM1P5A	N5	SPI1_MI
AD30	DVDD_SRAM_MODEM	AR7	EMI1_EXTR	N7	DVDD_CORE
AD31	MIPI2_D_SCLK	AR8	SCL2	N9	DVDD_CORE
AD32	MIPI2_D_SDATA	AR9	VDD2_EMI_B	P1	KPCOL1
AD33	MSDC1_DAT0	B1	NC_BGA_B1	P10	DVSS
AD34	MIPI_M_SCLK	B10	MSDC0_DAT0	P12	DVSS
AD35	MIPI_M_SDATA	B11	MSDC0_DAT4	P14	DVSS
AD4	CSI2B_L0N_T0B	B13	UFS_TX1N	P16	DVSS
AD5	CSI2B_L0P_T0A	B14	DVSS	P17	TP_APPLLGP
AD6	DVDD_GPU	B17	UFS_RX0P	P18	DVDD_PROC_B
AD7	DVDD_GPU	B18	UFS_RX0N	P19	DVSS
AE1	CSI2B_L1N_T1A	B19	DVSS	P2	KPROW0
AE11	DVDD_GPU	B2	DVSS	P20	DVDD_PROC_B
AE12	DVDD_GPU	B20	EMI0_ZQ0	P21	DVDD_PROC_B
AE16	DVDD_GPU	B21	VDD2_EMI_T	P22	DVSS
AE17	DVSS	B22	SRCLKENA1	P23	DVSS
AE19	DVDD_MODEM	B23	SCP_VREQ_VAO	P24	DVDD_PROC_B
AE2	CSI2B_L1P_T0C	B24	AUD_DAT_MOSI1	P25	DVDD_APU
AE21	DVDD_MODEM	B25	AUD_DAT_MOSI2	P26	DVDD_APU
AE23	DVDD_MODEM	B26	DVSS	P29	DVDD_APU
AE25	DVDD_MODEM	B27	AUD_DAT_MISO2	P3	KPROW1
AE26	DVDD_SRAM_MODEM	B28	SCL6	P30	DVDD_APU
AE27	DVDD_SRAM_MODEM	B29	SDA5	P31	DSI1_CKN_T1C
AE28	DVDD_SRAM_MODEM	B3	DVSS	P32	DSI1_CKP_T1B
AE29	DVDD_MODEM	B30	EINT22	P33	DSI1_D0N_T1A
AE3	DVSS	B31	EINT21	P34	DSI1_D1P_T2A

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AE30	DVDD_MODEM	B32	DVSS	P35	DSI1_D1N_T2B
AE31	MD_UCNT	B33	PERIPHERAL_EN4	P4	SPI1_CLK
AE32	DVSS	B34	VDD1_EMI_T	P5	SPI1_CSB
AE33	DVSS	B35	NC_BGA_B35	P6	DVSS
AE34	DVSS	B5	WF0_IP	P8	DVSS
AE35	DVSS	B7	WF1_IP	R1	EINT11
AE4	CSI2B_L2N_T1C	B9	VDD2_EMI_T	R11	DVSS
AE5	CSI2B_L2P_T1B	C1	VDDQ_EMI_T	R13	DVSS
AE6	DVDD_GPU	C11	MSDC0_DSL	R15	DVSS
AE7	DVDD_GPU	C12	DVSS	R17	TN_APPLLGP
AF1	CSI1A_L0N_T0B	C13	UFS_TX1P	R18	DVDD_PROC_B
AF11	DVSS	C15	UFS_TX0P	R19	DVSS
AF12	DVSS	C16	DVSS	R2	EINT10
AF16	DVSS	C18	DVSS	R23	DVSS
AF17	DVSS	C20	EMI0_ZQ1	R24	DVDD_PROC_B
AF18	DVSS	C21	PWRAP_SPI0_CK	R25	DVSS
AF19	DVSS	C22	WATCHDOG	R26	DVSS
AF2	CSI1A_L0P_T0A	C23	AUD_DAT_MOSI0	R27	DVSS
AF20	DVSS	C24	AUD_SYNC_MOSI	R28	DVSS
AF22	DVSS	C25	AUD_NLE_MOSI1	R29	DVSS
AF24	DVSS	C26	AUD_DAT_MISO0	R3	KPCOL0
AF26	DVSS	C27	AUD_NLE_MOSI0	R30	DVSS
AF27	DVDD_SRAM_MODEM	C28	SDA6	R31	DSI1_D2N_T0B
AF28	DVSS	C29	SDA0	R32	DSI1_D0P_T0C
AF3	CSI1A_L1P_T0C	C3	BT_IP	R33	DVSS
AF30	DVDD18_MSDC1	C30	EINT25	R34	AVDD04_DSI
AF31	DVSS	C31	EINT24	R35	AVDD12_DSI
AF32	DVSS	C32	PERIPHERAL_EN7	R4	EINT16
AF33	DRF_UL_LN1_DP	C33	PERIPHERAL_EN5	R5	EINT17
AF34	DRF_UL_LN1_DN	C34	PERIPHERAL_EN6	R7	DVSS
AF35	DRF_UL_LN0_DN	C35	VDDQ_EMI_T	R9	DVSS
AF4	CSI1A_L1N_T1A	C4	WF0_QN	T1	EINT14
AF5	DVSS	C5	DVSS	T10	DVDD_CORE
AF6	DVSS	C6	WF1_QP	T12	DVDD_CORE
AF7	DVSS	C7	DVSS	T14	DVDD_CORE
AG1	CSI1A_L2N_T1C	C8	DVDD18_MSDC0	T16	DVDD_CORE
AG10	DVSS	C9	MSDC0_DAT2	T17	AVDD12_APPLLGP
AG11	DVSS	D1	VDD2_EMI_T	T18	DVDD_PROC_B
AG12	DVSS	D11	MSDC0_DAT3	T19	DVSS
AG13	DVSS	D13	DVSS	T2	EINT13
AG14	DVSS	D15	UFS_TX0N	T23	DVSS
AG15	DVSS	D17	UFS_RX1P	T24	DVDD_PROC_B
AG16	DVSS	D18	UFS_RX1N	T25	DVDD_APU

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AG17	DVSS	D19	DVSS	T26	DVDD_APU
AG19	DVSS	D2	DVSS	T27	DVDD_APU
AG2	CSI1A_L2P_T1B	D20	PWRAP_SPI0_MO	T28	DVDD_APU
AG20	DVSS	D21	PWRAP_SPI0_CSN	T29	DVDD_APU
AG21	DVSS	D22	PWRAP_SPI0_MI	T3	EINT12
AG23	DVSS	D23	SRCLKENA0	T30	DVDD_APU
AG25	DVSS	D25	DVSS	T31	DSI1_D2P_T0A
AG27	DVSS	D29	SCL0	T32	DVSS
AG29	DVSS	D3	BT_IN	T33	DVSS
AG3	DVSS	D30	EINT23	T34	AVDD12_USB
AG30	DVSS	D31	PERIPHERAL_EN8	T35	AVDD12_SSUSB
AG31	DRF_UL_CP	D32	I2S3_BCK	T4	CAM_PDN2
AG32	DRF_UL_CN	D33	I2S3_LRCK	T5	CAM_CLK2
AG33	DVSS	D34	DVSS	T6	DVDD_CORE
AG34	DVSS	D35	VDD2_EMI_T	T8	DVDD_CORE
AG35	DRF_UL_LN0_DP	D4	WF0_QP	U1	CAM_PDN1
AG4	CSI1B_L0P_T0A	D5	DVSS	U11	DVDD_CORE
AG5	CSI1B_L0N_T0B	D6	WF1_QN	U13	DVDD_CORE
AG6	DVSS	D8	MSDC0_DAT7	U15	DVDD_CORE
AG7	DVSS	D9	MSDC0_DAT6	U17	AVDD18_APPLLGP
AG8	DVSS	E1	DVSS	U18	DVDD_PROC_B
AG9	DVSS	E10	MSDC0_DAT5	U19	DVSS
AH1	CSI1B_L1P_T0C	E11	MSDC0_RSTB	U2	CAM_CLK1
AH10	DVDD_GPU	E12	MSDC0_CLK	U20	DVSS
AH11	DVDD_GPU	E13	MSDC0_CMD	U21	DVDD_PROC_B
AH12	DVDD_GPU	E14	UFS_PLL_CKREF	U22	DVSS
AH13	DVDD_GPU	E16	UFS_REFCK_OUT	U23	DVSS
AH14	DVDD_GPU	E17	DVSS	U24	DVDD_PROC_B
AH15	DVDD_GPU	E18	DVSS	U25	DVSS
AH16	DVDD_MODEM	E19	DVSS	U26	DVSS
AH18	DVDD_MODEM	E2	BT_QN	U27	DVSS
AH2	CSI1B_L1N_T1A	E20	RTC32K_CK	U28	DVSS
AH20	DVDD_MODEM	E25	DVDD18_IOTM	U29	DVDD_CORE
AH22	DVDD_MODEM	E3	BT_QP	U3	EINT15
AH24	DVDD_MODEM	E32	I2S0_DI	U30	DVSS
AH26	DVDD_MODEM	E33	I2S3_DO	U31	DVSS
AH28	DVDD_MODEM	E34	I2S3_MCK	U32	AVDD18_USB
AH3	DVSS	E35	DVSS	U33	DVSS
AH30	DVDD_SRAM_MODEM	E4	DVSS	U34	SSUSB_TXP
AH31	DVSS	E5	AVDD18_WBG	U35	SSUSB_TXN
AH32	DRF_DL_CP	E6	DVSS	U4	CAM_RST2
AH33	DVSS	E8	DVSS	U5	CAM_PDN0
AH34	DVSS	E9	MSDC0_DAT1	U7	DVDD_CORE

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AH35	AVDD12_DRF	F1	GPS_I_L1	U9	DVDD_CORE
AH4	CSI1B_L2P_T1B	F10	AVDDQ_EMI0	V1	DVDD28_MSDC2
AH5	DVSS	F11	AVDD12_EMI0	V10	DVSS
AH6	DVDD_GPU	F13	DVSS	V12	DVSS
AH7	DVDD_GPU	F15	DVDD_ADSP	V14	DVSS
AH8	DVDD_GPU	F16	AVDD12_UFS	V15	DVDD_SRAM_CORE
AH9	DVDD_GPU	F18	DVDD_PROC_B	V16	DVDD_SRAM_CORE
AJ1	CSI0A_L0P_T0A	F19	DVSS	V18	DVSS
AJ10	DVSS	F2	GPS_Q_L1	V2	DVSS
AJ11	DVSS	F20	DVSS	V20	DVSS
AJ12	DVSS	F21	DVDD_PROC_B	V22	DVDD_MODEM
AJ13	DVDD_GPU	F22	DVDD_PROC_B	V24	DVDD_MODEM
AJ14	DVSS	F23	DVSS	V26	DVDD_NR
AJ15	DVDD_GPU	F24	DVDD_PROC_B	V27	DVDD_NR
AJ16	DVSS	F25	AVDD18_EMI2	V28	DVDD_NR
AJ17	DVDD_MODEM	F26	AVDD12_EMI2	V29	DVDD_NR
AJ19	DVDD_MODEM	F27	AVDDQ_EMI2	V3	CAM_RST1
AJ2	CSI0A_L0N_T0B	F28	AVDD075_EMI2	V30	DVDD_NR
AJ21	DVDD_MODEM	F29	AVDD075_EMI2	V31	SSUSB_RXP
AJ23	DVSS	F3	DVSS	V32	SSUSB_RXN
AJ24	DVDD_CORE	F30	AVDDQ_EMI2	V33	AUXIN4
AJ25	DVSS	F31	SPI5_MI	V34	AUXIN3
AJ27	DVSS	F32	SPI5_MO	V35	AVDD33_USB
AJ29	DVSS	F33	SPI5_CSB	V4	CAM_CLK0
AJ3	DVSS	F34	SPI5_CLK	V5	DVDD_GPU
AJ30	DVDD_MODEM	F35	DVDD18_IOLT	V6	DVSS
AJ31	DVSS	F5	AVDD12_WBG	V7	DVDD_SRAM_GPU
AJ32	DRF_DL_CN	F6	AVDDQ_EMI0	V8	DVDD_SRAM_GPU
AJ33	DVSS	F7	AVDD075_EMI0	V9	DVSS
AJ34	DVSS	F8	AVDDQ_EMI0	W1	CSI3A_L0P_T0A
AJ35	AVDD18_DRF	F9	AVDD075_EMI0	W10	DVSS
AJ4	CSI1B_L2N_T1C	G1	DVSS	W11	DVSS
AJ5	DVSS	G11	AVDD18_EMI0	W13	DVSS
AJ6	DVSS	G12	EMI0_EXTR	W15	DVSS
AJ7	DVSS	G13	DVSS	W17	DVSS
AJ9	DVDD_CORE	G14	DVSS	W19	DVSS
AK1	CSI0A_L2N_T1C	G15	DVDD_ADSP	W2	CSI3A_L0N_T0B
AK10	AVDD12_EMI1	G16	DVDD_ADSP	W21	DVSS
AK11	AVDD18_EMI1	G17	DVSS	W23	DVSS
AK12	DVSS	G18	DVDD_PROC_B	W25	DVSS
AK14	DVSS	G19	DVSS	W27	DVSS
AK15	DVSS	G2	GPS_I_L5	W29	DVSS
AK16	DVDD_CORE	G23	DVSS	W3	DVDD18_IORM

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AK17	DVSS	G24	DVDD_PROC_B	W30	DVSS
AK18	DVSS	G25	DVSS	W31	AUXIN2
AK19	DVSS	G26	DVSS	W32	AUXIN5
AK2	CSI0A_L2P_T1B	G27	DVSS	W33	USB_DP
AK20	DVSS	G28	DVDD_CORE	W34	USB_DM
AK21	AVDD12_MDPLLGP	G29	DVSS	W35	REFP
AK22	AVDD18_MDPLLGP	G3	GPS_Q_L5	W4	CAM_RST0
AK23	AVDD18_EMI3	G30	AVDDQ_EMI2	W5	DVSS
AK24	AVDD12_EMI3	G31	INT_SIM2	W6	DVSS
AK25	AVDDQ_EMI3	G32	SYSRSTB	W7	DVSS
AK26	AVDD075_EMI3	G33	LCM_RST	W8	DVSS
AK27	AVDDQ_EMI3	G34	DSI_TE	W9	DVDD_GPU
AK28	AVDD075_EMI3	G35	DISP_PWM	Y1	CSI3A_L1N_T1A
AK29	AVDDQ_EMI3	G4	DVSS	Y10	DVDD_CORE
AK3	CSI0A_L1N_T1A	G5	XIN_WBG	Y11	DVSS
AK30	DVDD_MODEM	G7	DVSS	Y12	DVDD_CORE
AK31	DRF_DL_LN2_DN	G8	DVSS	Y13	DVSS
AK32	DRF_DL_LN2_DP	G9	DVDD_CORE	Y14	DVDD_CORE
AK33	DRF_DL_LN1_DN	H1	CONN_WF_CTRL0	Y15	DVSS
AK34	DRF_DL_LN1_DP	H10	DVDD_CORE	Y16	DVDD_CORE
AK35	DRF_DL_LN0_DP	H12	DVDD_CORE	Y17	DVSS
AK4	CSI0A_L1P_T0C	H14	DVDD_CORE	Y18	DVDD_CORE
AK5	AVDDQ_EMI1	H15	DVDD_CORE	Y2	CSI3A_L1P_T0C
AK6	AVDD075_EMI1	H16	DVSS	Y20	DVDD_CORE
AK7	AVDDQ_EMI1	H17	DVSS	Y22	DVDD_MODEM
AK8	AVDD075_EMI1	H18	DVDD_PROC_B	Y24	DVDD_MODEM
AK9	AVDDQ_EMI1	H19	DVSS	Y26	DVDD_NR
AL1	CSI0B_L0P_T0A	H2	DVSS	Y28	DVDD_NR
AL13	SDA7	H23	DVSS	Y3	CSI3A_L2P_T1B
AL14	SCL9	H24	DVDD_PROC_B	Y30	DP_LN0_TXP
AL15	DVDD18_IOBM	H25	DVDD_DLA	Y31	DVSS
AL2	CSI0B_L0N_T0B	H26	DVDD_DLA	Y32	AUXIN0
AL24	DVDD_CORE	H28	DVDD_DLA	Y33	AUXIN1
AL25	BPI_D_BUS20_ANT3	H3	DVSS	Y34	DVSS
AL26	BPI_D_BUS13_OLAT2	H30	DVDD_DLA	Y35	AVDD12_DPTX
AL27	MIPI1_D_SDATA	H31	DVDD18_SIM2	Y4	DVDD18_MSDC2
AL28	MIPI0_D_SDATA	H32	INT_SIM1	Y5	DVDD_GPU
AL3	DVSS	H33	SIM2_SRST	Y6	DVDD_GPU
AL31	DVSS	H34	SIM2_SCLK	Y7	DVSS
AL32	DVSS	H35	SIM2_SIO	Y8	DVDD_GPU
AL33	DVSS	H4	DVDD_CORE	Y9	DVDD_GPU
AL35	DRF_DL_LN0_DN	H5	DVSS		
AL4	CSI0B_L1P_T0C	H6	DVDD_CORE		

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AL6	DVSS	H8	DVDD_CORE		
AM1	CSI0B_L2N_T1C	J1	CONN_HRST_B		
AM10	EINT9	J11	DVDD_CORE		
AM11	EINT2	J13	DVDD_CORE		
AM12	EINT7	J15	DVSS		

Table 2-2. TOP ball pin coordinate LPDDR4X

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	G14	DVSS	AC20	DVSS
A2	VDD2_EMI_T	G15	DVSS	AC21	DVSS
A3	DVSS	G16	DVSS	AC22	DVSS
A4	VDDQ_EMI_T	G17	DVSS	AC23	DVSS
A5	VDD1_EMI_T	G18	DVSS	AC24	DVSS
A6	VDD2_EMI_T	G19	DVSS	AC25	DVSS
A7	EMI0_CS0	G20	DVSS	AC26	DVSS
A8	VDD2_EMI_T	G21	DVSS	AC27	DVSS
A9	DVSS	G22	DVSS	AC28	DVSS
A10	VDD2_EMI_T	G23	DVSS	AC29	DVSS
A11	VDDQ_EMI_T	G24	DVSS	AD1	VDD2_EMI_B
A12	DVSS	G25	DVSS	AD2	VDD2_EMI_B
A13	VDDQ_EMI_T	G26	DVSS	AD3	DVSS
A14	VDD2_EMI_T	G27	DVSS	AD4	DVSS
A15	DVSS	G28	DVSS	AD5	DVSS
A16	VDD2_EMI_T	G29	DVSS	AD6	DVSS
A17	VDDQ_EMI_T	H1	NC	AD7	DVSS
A18	DVSS	H2	NC	AD8	DVSS
A19	VDDQ_EMI_T	H3	DVSS	AD9	DVSS
A20	VDD2_EMI_T	H4	DVSS	AD10	DVSS
A21	DVSS	H5	DVSS	AD11	DVSS
A22	VDD2_EMI_T	H25	DVSS	AD12	DVSS
A23	EMI2_CS0	H26	DVSS	AD13	DVSS
A24	VDD2_EMI_T	H27	DVSS	AD14	DVSS
A25	VDD1_EMI_T	H28	NC	AD15	DVSS
A26	VDDQ_EMI_T	H29	NC	AD16	DVSS
A27	DVSS	J1	NC	AD17	DVSS
A28	VDD2_EMI_T	J2	NC	AD18	DVSS
A29	NC	J3	DVSS	AD19	DVSS
B1	VDD1_EMI_T	J4	DVSS	AD20	DVSS
B2	EMI0_DQ2	J5	DVSS	AD21	DVSS
B3	EMI0_DQS0_T	J25	DVSS	AD22	DVSS
B4	EMI0_DQ4	J26	DVSS	AD23	DVSS
B5	DVSS	J27	DVSS	AD24	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
B6	EMI0_CA0	J28	NC	AD25	DVSS
B7	EMI0_CS1	J29	NC	AD26	DVSS
B8	EMI0_CK_T	K1	NC	AD27	DVSS
B9	EMI0_CA3	K2	NC	AD28	VDD2_EMI_B
B10	VDD1_EMI_T	K3	DVSS	AD29	VDD2_EMI_B
B11	EMI0_DQ13	K4	DVSS	AE1	EMI1_DQ1
B12	EMI0_DQS1_T	K5	DVSS	AE2	DVSS
B13	EMI0_DQ11	K25	DVSS	AE3	EMI1_DMI0
B14	VDD1_EMI_T	K26	DVSS	AE4	DVSS
B15	NC	K27	DVSS	AE5	EMI1_DQ7
B16	VDD1_EMI_T	K28	NC	AE6	VDD2_EMI_B
B17	EMI2_DQ11	K29	NC	AE7	EMI1_CKE1
B18	EMI2_DQS1_T	L1	NC	AE8	EMI1_CA2
B19	EMI2_DQ13	L2	NC	AE9	EMI1_CA5
B20	VDD1_EMI_T	L3	DVSS	AE10	EMI1_DQ14
B21	EMI2_CA3	L4	DVSS	AE11	DVSS
B22	EMI2_CK_T	L5	DVSS	AE12	EMI1_DMI1
B23	EMI2_CS1	L25	DVSS	AE13	DVSS
B24	EMI2_CA0	L26	DVSS	AE14	EMI1_DQ8
B25	DVSS	L27	DVSS	AE15	EMI3_ZQ0
B26	EMI2_DQ4	L28	NC	AE16	EMI3_DQ8
B27	EMI2_DQS0_T	L29	NC	AE17	DVSS
B28	EMI2_DQ2	M1	NC	AE18	EMI3_DMI1
B29	VDD1_EMI_T	M2	NC	AE19	DVSS
C1	EMI0_DQ0	M3	DVSS	AE20	EMI3_DQ14
C2	DVSS	M4	DVSS	AE21	EMI3_CA5
C3	EMI0_DQS0_C	M5	DVSS	AE22	EMI3_CA2
C4	DVSS	M25	DVSS	AE23	EMI3_CKE1
C5	EMI0_DQ6	M26	DVSS	AE24	VDD2_EMI_B
C6	DVSS	M27	DVSS	AE25	EMI3_DQ7
C7	VDD2_EMI_T	M28	NC	AE26	DVSS
C8	EMI0_CK_C	M29	NC	AE27	EMI3_DMI0
C9	VDD2_EMI_T	N1	NC	AE28	DVSS
C10	EMI0_DQ15	N2	NC	AE29	EMI3_DQ1
C11	DVSS	N3	DVSS	AF1	VDDQ_EMI_B
C12	EMI0_DQS1_C	N4	DVSS	AF2	EMI1_DQ3
C13	DVSS	N5	DVSS	AF3	VDDQ_EMI_B
C14	EMI0_DQ9	N25	DVSS	AF4	EMI1_DQ5
C15	EMI0_RESET_N	N26	DVSS	AF5	VDDQ_EMI_B
C16	EMI2_DQ9	N27	DVSS	AF6	EMI1_CA1
C17	DVSS	N28	NC	AF7	EMI1_CKE0
C18	EMI2_DQS1_C	N29	NC	AF8	DVSS
C19	DVSS	P1	NC	AF9	EMI1_CA4

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C20	EMI2_DQ15	P2	NC	AF10	VDDQ_EMI_B
C21	VDD2_EMI_T	P3	DVSS	AF11	EMI1_DQ12
C22	EMI2_CK_C	P4	DVSS	AF12	VDDQ_EMI_B
C23	VDD2_EMI_T	P5	DVSS	AF13	EMI1_DQ10
C24	DVSS	P25	DVSS	AF14	VDDQ_EMI_B
C25	EMI2_DQ6	P26	DVSS	AF15	EMI3_ZQ1
C26	DVSS	P27	DVSS	AF16	VDDQ_EMI_B
C27	EMI2_DQS0_C	P28	NC	AF17	EMI3_DQ10
C28	DVSS	P29	NC	AF18	VDDQ_EMI_B
C29	EMI2_DQ0	R1	NC	AF19	EMI3_DQ12
D1	VDDQ_EMI_T	R2	NC	AF20	VDDQ_EMI_B
D2	EMI0_DQ3	R3	DVSS	AF21	EMI3_CA4
D3	VDDQ_EMI_T	R4	DVSS	AF22	DVSS
D4	EMI0_DQ5	R5	DVSS	AF23	EMI3_CKE0
D5	VDDQ_EMI_T	R25	DVSS	AF24	EMI3_CA1
D6	EMI0_CA1	R26	DVSS	AF25	VDDQ_EMI_B
D7	EMI0_CKE0	R27	DVSS	AF26	EMI3_DQ5
D8	DVSS	R28	NC	AF27	VDDQ_EMI_B
D9	EMI0_CA4	R29	NC	AF28	EMI3_DQ3
D10	VDDQ_EMI_T	T1	NC	AF29	VDDQ_EMI_B
D11	EMI0_DQ12	T2	NC	AG1	EMI1_DQ0
D12	VDDQ_EMI_T	T3	DVSS	AG2	DVSS
D13	EMI0_DQ10	T4	DVSS	AG3	EMI1_DQS0_C
D14	VDDQ_EMI_T	T5	DVSS	AG4	DVSS
D15	EMI0_ZQ1	T25	DVSS	AG5	EMI1_DQ6
D16	VDDQ_EMI_T	T26	DVSS	AG6	DVSS
D17	EMI2_DQ10	T27	DVSS	AG7	VDD2_EMI_B
D18	VDDQ_EMI_T	T28	NC	AG8	EMI1_CK_C
D19	EMI2_DQ12	T29	NC	AG9	VDD2_EMI_B
D20	VDDQ_EMI_T	U1	NC	AG10	EMI1_DQ15
D21	EMI2_CA4	U2	NC	AG11	DVSS
D22	DVSS	U3	DVSS	AG12	EMI1_DQS1_C
D23	EMI2_CKE0	U4	DVSS	AG13	DVSS
D24	EMI2_CA1	U5	DVSS	AG14	EMI1_DQ9
D25	VDDQ_EMI_T	U25	DVSS	AG15	NC
D26	EMI2_DQ5	U26	DVSS	AG16	EMI3_DQ9
D27	VDDQ_EMI_T	U27	DVSS	AG17	DVSS
D28	EMI2_DQ3	U28	NC	AG18	EMI3_DQS1_C
D29	VDDQ_EMI_T	U29	NC	AG19	DVSS
E1	EMI0_DQ1	V1	NC	AG20	EMI3_DQ15
E2	DVSS	V2	NC	AG21	VDD2_EMI_B
E3	EMI0_DMI0	V3	DVSS	AG22	EMI3_CK_C
E4	DVSS	V4	DVSS	AG23	VDD2_EMI_B

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
E5	EMI0_DQ7	V5	DVSS	AG24	DVSS
E6	VDD2_EMI_T	V25	DVSS	AG25	EMI3_DQ6
E7	EMI0_CKE1	V26	DVSS	AG26	DVSS
E8	EMI0_CA2	V27	DVSS	AG27	EMI3_DQS0_C
E9	EMI0_CA5	V28	NC	AG28	DVSS
E10	EMI0_DQ14	V29	NC	AG29	EMI3_DQ0
E11	DVSS	W1	NC	AH1	VDD1_EMI_B
E12	EMI0_DMI1	W2	NC	AH2	EMI1_DQ2
E13	DVSS	W3	DVSS	AH3	EMI1_DQS0_T
E14	EMI0_DQ8	W4	DVSS	AH4	EMI1_DQ4
E15	EMI0_ZQ0	W5	DVSS	AH5	DVSS
E16	EMI2_DQ8	W25	DVSS	AH6	EMI1_CA0
E17	DVSS	W26	DVSS	AH7	EMI1_CS1
E18	EMI2_DMI1	W27	DVSS	AH8	EMI1_CK_T
E19	DVSS	W28	NC	AH9	EMI1_CA3
E20	EMI2_DQ14	W29	NC	AH10	VDD1_EMI_B
E21	EMI2_CA5	Y1	NC	AH11	EMI1_DQ13
E22	EMI2_CA2	Y2	NC	AH12	EMI1_DQS1_T
E23	EMI2_CKE1	Y3	DVSS	AH13	EMI1_DQ11
E24	VDD2_EMI_T	Y4	DVSS	AH14	VDD1_EMI_B
E25	EMI2_DQ7	Y5	DVSS	AH15	NC
E26	DVSS	Y25	DVSS	AH16	VDD1_EMI_B
E27	EMI2_DMI0	Y26	DVSS	AH17	EMI3_DQ11
E28	DVSS	Y27	DVSS	AH18	EMI3_DQS1_T
E29	EMI2_DQ1	Y28	NC	AH19	EMI3_DQ13
F1	VDD2_EMI_T	Y29	NC	AH20	VDD1_EMI_B
F2	VDD2_EMI_T	AA1	NC	AH21	EMI3_CA3
F3	DVSS	AA2	NC	AH22	EMI3_CK_T
F4	DVSS	AA3	DVSS	AH23	EMI3_CS1
F5	DVSS	AA4	DVSS	AH24	EMI3_CA0
F6	DVSS	AA5	DVSS	AH25	DVSS
F7	DVSS	AA25	DVSS	AH26	EMI3_DQ4
F8	DVSS	AA26	DVSS	AH27	EMI3_DQS0_T
F9	DVSS	AA27	DVSS	AH28	EMI3_DQ2
F10	DVSS	AA28	NC	AH29	VDD1_EMI_B
F11	DVSS	AA29	NC	AJ1	NC
F12	DVSS	AB1	NC	AJ2	VDD2_EMI_B
F13	DVSS	AB2	NC	AJ3	DVSS
F14	DVSS	AB3	DVSS	AJ4	VDDQ_EMI_B
F15	DVSS	AB4	DVSS	AJ5	VDD1_EMI_B
F16	DVSS	AB5	DVSS	AJ6	VDD2_EMI_B
F17	DVSS	AB25	DVSS	AJ7	EMI1_CS0
F18	DVSS	AB26	DVSS	AJ8	VDD2_EMI_B

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
F19	DVSS	AB27	DVSS	AJ9	DVSS
F20	DVSS	AB28	NC	AJ10	VDD2_EMI_B
F21	DVSS	AB29	NC	AJ11	VDDQ_EMI_B
F22	DVSS	AC1	DVSS	AJ12	DVSS
F23	DVSS	AC2	DVSS	AJ13	VDDQ_EMI_B
F24	DVSS	AC3	DVSS	AJ14	VDD2_EMI_B
F25	DVSS	AC4	DVSS	AJ15	DVSS
F26	DVSS	AC5	DVSS	AJ16	VDD2_EMI_B
F27	DVSS	AC6	DVSS	AJ17	VDDQ_EMI_B
F28	VDD2_EMI_T	AC7	DVSS	AJ18	DVSS
F29	VDD2_EMI_T	AC8	DVSS	AJ19	VDDQ_EMI_B
G1	DVSS	AC9	DVSS	AJ20	VDD2_EMI_B
G2	DVSS	AC10	DVSS	AJ21	DVSS
G3	DVSS	AC11	DVSS	AJ22	VDD2_EMI_B
G4	DVSS	AC12	DVSS	AJ23	EMI3_CS0
G5	DVSS	AC13	DVSS	AJ24	VDD2_EMI_B
G6	DVSS	AC14	DVSS	AJ25	VDD1_EMI_B
G7	DVSS	AC15	DVSS	AJ26	VDDQ_EMI_B
G8	DVSS	AC16	DVSS	AJ27	DVSS
G9	DVSS	AC17	DVSS	AJ28	VDD2_EMI_B
G10	DVSS	AC18	DVSS	AJ29	NC
G11	DVSS	AC19	DVSS		
G12	DVSS				
G13	DVSS				

2.1.3 Detailed Pin Description

Table 2-3. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

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Table 2-4. Detailed pin description

Pin name	Pin no.	Type	Description	Power domain
System				
SYSRSTB	G32	DI	System reset input	DVDD18
WATCHDOG	C22	DIO	Watchdog reset output	DVDD18
TESTMODE	AM25	DI	Test mode	DVDD18
RTC32K_CK	E20	DIO	RTC 32K input	DVDD18
SRCLKENA0	D23	DIO	Output signal; control 26 Hz/Buck/LDO normal mode or sleep mode. (High: normal mode; low: sleep mode or low power mode)	DVDD18
SRCLKENA1	B22	DIO	Output signal; control VRF18. (High: VRF18 on; low: VRF18 off)	DVDD18
AP_GOOD	AN25	DIO	When bootrom can normally jump into pre-loader execution (i.e. software can take over), bootrom makes AP_GOOD high before jumping.	DVDD18
EINT0	AP13	DIO	External interrupt input	DVDD18
EINT1	AN12	DIO	External interrupt input	DVDD18
EINT2	AM11	DIO	External interrupt input	DVDD18
EINT3	AN13	DIO	External interrupt input	DVDD18
EINT4	AP11	DIO	External interrupt input	DVDD18
EINT5	AN11	DIO	External interrupt input	DVDD18
EINT6	AR11	DIO	External interrupt input	DVDD18
EINT7	AM12	DIO	External interrupt input	DVDD18
EINT8	AP12	DIO	External interrupt input	DVDD18
EINT9	AM10	DIO	External interrupt input	DVDD18
EINT10	R2	DIO	External interrupt input	DVDD18
EINT11	R1	DIO	External interrupt input	DVDD18
EINT12	T3	DIO	External interrupt input	DVDD18
EINT13	T2	DIO	External interrupt input	DVDD18
EINT14	T1	DIO	External interrupt input	DVDD18
EINT15	U3	DIO	External interrupt input	DVDD18
EINT16	R4	DIO	External interrupt input	DVDD18
PMIC				
PWRAP_SPI0_MO	D20	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_MI	D22	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CSN	D21	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CK	C21	DIO	PMIC SPI control interface	DVDD18
AUD_DAT_MISO1	A28	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO0	C26	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI0	C23	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI1	B24	DIO	PMIC audio input interface	DVDD18
AUD_NLE_MOSI1	C25	DIO	PMIC audio input interface	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
AUD_DAT_MISO2	B27	DIO	PMIC audio input interface	DVDD18
AUD_NLE_MOSI0	C27	DIO	PMIC audio input interface	DVDD18
AUD_CLK_MOSI	A25	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MOSI	C24	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI2	B25	DIO	PMIC audio input interface	DVDD18
SCP_VREQ_VAO	B23	DIO	SCP to PMIC normal voltage request	DVDD18
SIM				
SIM1_SCLK	J34	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	J33	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	J35	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	H34	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	H35	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	H33	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	H32	DIO	SIM1 interrupt	DVDD18
INT_SIM2	G31	DIO	SIM2 interrupt	DVDD18
I2S				
I2S0_DI	E32	DIO	I2S interface	DVDD18
I2S1_BCK	AM18	DIO	I2S interface	DVDD18
I2S1_DO	AM17	DIO	I2S interface	DVDD18
I2S1_LRCK	AR17	DIO	I2S interface	DVDD18
I2S1_MCK	AP18	DIO	I2S interface	DVDD18
I2S2_DI	AN18	DIO	I2S interface	DVDD18
I2S3_BCK	D32	DIO	I2S interface	DVDD18
I2S3_DO	E33	DIO	I2S interface	DVDD18
I2S3_LRCK	D33	DIO	I2S interface	DVDD18
I2S3_MCK	E34	DIO	I2S interface	DVDD18
LCD				
DSI_TE	G34	DIO	Parallel display interface tearing effect	DVDD18
LCM_RST	G33	DIO	Parallel display interface reset signal	DVDD18
PWM				
DISP_PWM	G35	DIO	Display PWM output	DVDD18
Keypad interface				
KPCOL0	R3	DIO	Keypad column 0	DVDD18
KPCOL1	P1	DIO	Keypad column 1	DVDD18
KPROW0	P2	DIO	Keypad row 0	DVDD18
KPROW1	P3	DIO	Keypad row 1	DVDD18
SPI				
SPI0_CSB	AP19	DIO	SPI0 chip select	DVDD18
SPI0_MI	AP20	DIO	SPI0 data in	DVDD18
SPI0_MO	AN20	DIO	SPI0 data out	DVDD18
SPI0_CLK	AM20	DIO	SPI0 clock	DVDD18
SPI1_CSB	P5	DIO	SPI1 chip select	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
SPI1_MI	N5	DIO	SPI1 data in	DVDD18
SPI1_MO	N3	DIO	SPI1 data out	DVDD18
SPI1_CLK	P4	DIO	SPI1 clock	DVDD18
SPI5_CSB	F33	DIO	SPI5 chip select	DVDD18
SPI5_MI	F31	DIO	SPI5 data in	DVDD18
SPI5_MO	F32	DIO	SPI5 data out	DVDD18
SPI5_CLK	F34	DIO	SPI5 clock	DVDD18
UR				
UTXD0	AM24	DIO	UR0 interdace	DVDD18
URXD0	AN24	DIO	SPI0 data in	DVDD18
UTXD1	AN23	DIO	UR1 Tx	DVDD18
URXD1	AP23	DIO	UR1 Rx	DVDD18
RF interface				
BPI_D_BUS0	AP33	DIO	BPI_BUS0	DVDD18
BPI_D_BUS1	AN35	DIO	BPI_BUS1	DVDD18
BPI_D_BUS2	AN31	DIO	BPI_BUS2	DVDD18
BPI_D_BUS20_ANT3	AL25	DIO	BPI_BUS3	DVDD18
BPI_D_BUS21_ANT4	AM29	DIO	BPI_BUS4	DVDD18
BPI_D_BUS3	AN32	DIO	BPI_BUS5	DVDD18
BPI_D_BUS4	AM31	DIO	BPI_BUS6	DVDD18
BPI_D_BUS5	AR33	DIO	BPI_BUS7	DVDD18
BPI_D_BUS6	AN34	DIO	BPI_BUS8	DVDD18
BPI_D_BUS7	AM32	DIO	BPI_BUS9	DVDD18
BPI_D_BUS8	AP32	DIO	BPI_BUS10	DVDD18
BPI_D_BUS9	AR32	DIO	BPI_BUS11	DVDD18
BPI_D_BUS10	AP31	DIO	BPI_BUS12	DVDD18
BPI_D_BUS11_OLAT0	AN28	DIO	BPI_BUS13	DVDD18
BPI_D_BUS12_OLAT1	AP29	DIO	BPI_BUS14	DVDD18
BPI_D_BUS13_OLAT2	AL26	DIO	BPI_BUS15	DVDD18
BPI_D_BUS14_OLAT3	AN29	DIO	BPI_BUS16	DVDD18
BPI_D_BUS15_OLAT4	AN27	DIO	BPI_BUS17	DVDD18
BPI_D_BUS16_OLAT5	AP28	DIO	BPI_BUS18	DVDD18
BPI_D_BUS17_ANT0	AM28	DIO	BPI_BUS19	DVDD18
ANT_SEL0	K3	DIO	BPI control	DVDD18
ANT_SEL1	M1	DIO	BPI control	DVDD18
ANT_SEL2	L2	DIO	BPI control	DVDD18
ANT_SEL3	L3	DIO	BPI control	DVDD18
ANT_SEL4	L5	DIO	BPI control	DVDD18
ANT_SEL5	M2	DIO	BPI control	DVDD18
ANT_SEL6	M3	DIO	BPI control	DVDD18
ANT_SEL7	M5	DIO	BPI control	DVDD18
ANT_SEL8	M4	DIO	BPI control	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
ANT_SEL9	N4	DIO	BPI control	DVDD18
MD_UCNT	AE31	DIO	BPI control	DVDD18
BSI				
MIPI_M_SCLK	AD34	DIO	MIPI_M CLK	DVDD18
MIPI_M_SDATA	AD35	DIO	MIPI_M DATA	DVDD18
MIPI0_D_SCLK	AM27	DIO	MIPI_0 CLK	DVDD18
MIPI0_D_SDATA	AL28	DIO	MIPI_0 DATA	DVDD18
MIPI1_D_SCLK	AM26	DIO	MIPI_1 CLK	DVDD18
MIPI1_D_SDATA	AL27	DIO	MIPI_1 DATA	DVDD18
MIPI2_D_SCLK	AD31	DIO	MIPI_2 CLK	DVDD18
MIPI2_D_SDATA	AD32	DIO	MIPI_2 DATA	DVDD18
MSDC0				
MSDC0_CLK	E12	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	E13	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	B10	DIO	MSDC0 data 0 pin	DVDD18_MSDC0
MSDC0_DAT1	E9	DIO	MSDC0 data 1 pin	DVDD18_MSDC0
MSDC0_DAT2	C9	DIO	MSDC0 data 2 pin	DVDD18_MSDC0
MSDC0_DAT3	D11	DIO	MSDC0 data 3 pin	DVDD18_MSDC0
MSDC0_DAT4	B11	DIO	MSDC0 data 4 pin	DVDD18_MSDC0
MSDC0_DAT5	E10	DIO	MSDC0 data 5 pin	DVDD18_MSDC0
MSDC0_DAT6	D9	DIO	MSDC0 data 6 pin	DVDD18_MSDC0
MSDC0_DAT7	D8	DIO	MSDC0 data 7 pin	DVDD18_MSDC0
MSDC0_DSL	C11	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	E11	DIO	MSDC0 reset pin	DVDD18_MSDC0
MSDC1				
MSDC1_CLK	AC30	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	AC31	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	AD33	DIO	MSDC1 data 0 pin	DVDD28_MSDC1
MSDC1_DAT1	AC33	DIO	MSDC1 data 1 pin	DVDD28_MSDC1
MSDC1_DAT2	AC35	DIO	MSDC1 data 2 pin	DVDD28_MSDC1
MSDC1_DAT3	AC34	DIO	MSDC1 data 3 pin	DVDD28_MSDC1
eFuse				
DVDD18_VQPS	AB5	DIO	eFuse blowing power control	DVDD_VQPS
EMI				
EMI0_EXTR	G12	DIO	DRAM interface	AVDDQ_EMI
EMI1_EXTR	AR7	DIO	DRAM interface	AVDDQ_EMI
EMI2_EXTR	A33	DIO	DRAM interface	AVDDQ_EMI
EMI3_EXTR	AR20	DIO	DRAM interface	AVDDQ_EMI
EMI0_ZQ0	B20	DIO	DRAM interface	AVDDQ_EMI
EMI0_ZQ1	C20	DIO	DRAM interface	AVDDQ_EMI
EMI3_ZQ0	AR18	DIO	DRAM interface	AVDDQ_EMI
EMI3_ZQ1	AR19	DIO	DRAM interface	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
VDD1_EMI_B	AN1	DIO	DRAM power	VDD1_EMI
VDD1_EMI_B	AN1	DIO	DRAM power	VDD1_EMI
VDD1_EMI_B	AN1	DIO	DRAM power	VDD1_EMI
VDD1_EMI_B	AN1	DIO	DRAM power	VDD1_EMI
VDD1_EMI_T	A14	DIO	DRAM power	VDD1_EMI
VDD1_EMI_T	A14	DIO	DRAM power	VDD1_EMI
VDD1_EMI_T	A14	DIO	DRAM power	VDD1_EMI
VDD1_EMI_T	A14	DIO	DRAM power	VDD1_EMI
VDD1_EMI_T	A14	DIO	DRAM power	VDD1_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_B	AN3	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	DIO	DRAM power	VDD2_EMI
VDDQ_EMI_B	AP2	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AP2	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AP2	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AP2	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A15	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A15	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A15	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A15	DIO	DRAM power	VDDQ_EMI
AVDD075_EMI0	F7	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI0	F7	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI1	AK6	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI1	AK6	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI2	F28	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI2	F28	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI3	AK26	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI3	AK26	DIO	DRAM power	AVDD075_EMI
AVDD12_EMI0	F11	DIO	DRAM power	AVDD12_EMI

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Pin name	Pin no.	Type	Description	Power domain
AVDD12_EMI1	AK10	DIO	DRAM power	AVDD12_EMI
AVDD12_EMI2	F26	DIO	DRAM power	AVDD12_EMI
AVDD12_EMI3	AK24	DIO	DRAM power	AVDD12_EMI
AVDDQ_EMI0	F10	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI0	F10	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI0	F10	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI1	AK5	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI1	AK5	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI1	AK5	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI2	F27	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI2	F27	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI2	F27	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI3	AK25	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI3	AK25	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI3	AK25	DIO	DRAM power	AVDDQ_EMI
EMI0_EXTR	G12	DIO	DRAM interface	AVDDQ_EMI
EMI1_EXTR	AR7	DIO	DRAM interface	AVDDQ_EMI
EMI2_EXTR	A33	DIO	DRAM interface	AVDDQ_EMI
EMI3_EXTR	AR20	DIO	DRAM interface	AVDDQ_EMI
CAM				
CAM_CLK0	V4	DIO	Master clock to 0th sensor	DVDD18
CAM_CLK1	U2	DIO	Master clock to 1st sensor	DVDD18
CAM_CLK2	T5	DIO	Master clock to 2nd sensor	DVDD18
CAM_CLK3	AM6	DIO	Master clock to 3rd sensor	DVDD18
CAM_CLK4	AP5	DIO	Master clock to 4th sensor	DVDD18
CAM_CLK5	AR3	DIO	Master clock to 5th sensor	DVDD18
CAM_PDN0	U5	DIO	Power down to 0th sensor	DVDD18
CAM_PDN1	U1	DIO	Power down to 1st sensor	DVDD18
CAM_PDN2	T4	DIO	Power down to 2nd sensor	DVDD18
CAM_PDN3	AN5	DIO	Power down to 3rd sensor	DVDD18
CAM_PDN4	AR4	DIO	Power down to 4th sensor	DVDD18
CAM_PDN5	AP3	DIO	Power down to 5th sensor	DVDD18
CAM_RST0	W4	DIO	Reset control to 0th sensor	DVDD18
CAM_RST1	V3	DIO	Reset control to 1st sensor	DVDD18
CAM_RST2	U4	DIO	Reset control to 2nd sensor	DVDD18
CAM_RST3	AN6	DIO	Reset control to 3rd sensor	DVDD18
CAM_RST4	AR5	DIO	Reset control to 4th sensor	DVDD18
CAM_RST5	AP4	DIO	Reset control to 5th sensor	DVDD18
I2C				
SCL0	D29	DIO	I2C0 clock	DVDD18
SCL1	AM15	DIO	I2C1 clock	DVDD18
SCL2	AR8	DIO	I2C2 clock	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
SCL3	N2	DIO	I2C3 clock	DVDD18
SCL4	AN7	DIO	I2C4 clock	DVDD18
SCL5	A29	DIO	I2C5 clock	DVDD18
SCL6	B28	DIO	I2C6 clock	DVDD18
SCL7	AM13	DIO	I2C7 clock	DVDD18
SCL8	AP14	DIO	I2C8 clock	DVDD18
SCL9	AL14	DIO	I2C9 clock	DVDD18
SDA0	C29	DIO	I2C0 data	DVDD18
SDA1	AN15	DIO	I2C1 data	DVDD18
SDA2	AP8	DIO	I2C2 data	DVDD18
SDA3	N1	DIO	I2C3 data	DVDD18
SDA4	AP7	DIO	I2C4 data	DVDD18
SDA5	B29	DIO	I2C5 data	DVDD18
SDA6	C28	DIO	I2C6 data	DVDD18
SDA7	AL13	DIO	I2C7 data	DVDD18
SDA8	AN14	DIO	I2C8 data	DVDD18
SDA9	AM14	DIO	I2C9 data	DVDD18
CONN				
CONN_BT_CLK	K4	DIO	Connsys BT 2-wire interface	DVDD18
CONN_BT_DATA	J5	DIO	Connsys BT 2-wire interface	DVDD18
CONN_HRST_B	J1	DIO	Connsys reset	DVDD18
CONN_TOP_CLK	L4	DIO	Connsys Top 2-wire interface	DVDD18
CONN_TOP_DATA	K5	DIO	Connsys Top 2-wire interface	DVDD18
CONN_WB_PTA	J4	DIO	Connsys Wi-Fi/BT PTA	DVDD18
CONN_WF_CTRL0	H1	DIO	Connsys Wi-Fi 3-wire interface	DVDD18
CONN_WF_CTRL1	J3	DIO	Connsys Wi-Fi 3-wire interface	DVDD18
CONN_WF_CTRL2	K1	DIO	Connsys Wi-Fi 3-wire interface	DVDD18
CONN_WF_CTRL3	J2	DIO	Connsys Wi-Fi 3-wire interface	DVDD18
CONN_WF_CTRL4	K2	DIO	Connsys Wi-Fi 3-wire interface	DVDD18
SCP				
SCP_SPI2_CK	AN17	DIO	System companion processor clk	DVDD18
SCP_SPI2_CSB	AN16	DIO	System companion processor chip select	DVDD18
SCP_SPI2_MI	AP16	DIO	System companion processor datain	DVDD18
SCP_SPI2_MO	AP17	DIO	System bompanion processor dataout	DVDD18
SCP_VREQ_VAO	B23	DIO	System bompanion processor voltage request	DVDD18
DigRF				
DRF_DL_CN	AJ32	AIO	DRF interface	AVDD18_DRF
DRF_DL_CP	AH32	AIO	DRF interface	AVDD18_DRF
DRF_DL_LN0_DN	AL35	AIO	DRF interface	AVDD18_DRF
DRF_DL_LN0_DP	AK35	AIO	DRF interface	AVDD18_DRF
DRF_DL_LN1_DN	AK33	AIO	DRF interface	AVDD18_DRF

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Pin name	Pin no.	Type	Description	Power domain
DRF_DL_LN1_DP	AK34	AIO	DRF interface	AVDD18_DRF
DRF_DL_LN2_DN	AK31	AIO	DRF interface	AVDD18_DRF
DRF_DL_LN2_DP	AK32	AIO	DRF interface	AVDD18_DRF
DRF_UL_CN	AG32	AIO	DRF interface	AVDD18_DRF
DRF_UL_CP	AG31	AIO	DRF interface	AVDD18_DRF
DRF_UL_LN0_DN	AF35	AIO	DRF interface	AVDD18_DRF
DRF_UL_LN0_DP	AG35	AIO	DRF interface	AVDD18_DRF
DRF_UL_LN1_DN	AF34	AIO	DRF interface	AVDD18_DRF
DRF_UL_LN1_DP	AF33	AIO	DRF interface	AVDD18_DRF
MIPI				
DSI0_CKN_T1C	M31	AIO	DSI interface	AVDD12_DSI
DSI0_CKP_T1B	M32	AIO	DSI interface	AVDD12_DSI
DSI0_D0N_T1A	M34	AIO	DSI interface	AVDD12_DSI
DSI0_D0P_T0C	M35	AIO	DSI interface	AVDD12_DSI
DSI0_D1N_T2B	L34	AIO	DSI interface	AVDD12_DSI
DSI0_D1P_T2A	L35	AIO	DSI interface	AVDD12_DSI
DSI0_D2N_T0B	N32	AIO	DSI interface	AVDD12_DSI
DSI0_D2P_T0A	N31	AIO	DSI interface	AVDD12_DSI
DSI0_D3N	L31	AIO	DSI interface	AVDD12_DSI
DSI0_D3P_T2C	L32	AIO	DSI interface	AVDD12_DSI
DSI1_CKN_T1C	P31	AIO	DSI interface	AVDD12_DSI
DSI1_CKP_T1B	P32	AIO	DSI interface	AVDD12_DSI
DSI1_D0N_T1A	P33	AIO	DSI interface	AVDD12_DSI
DSI1_D0P_T0C	R32	AIO	DSI interface	AVDD12_DSI
DSI1_D1N_T2B	P35	AIO	DSI interface	AVDD12_DSI
DSI1_D1P_T2A	P34	AIO	DSI interface	AVDD12_DSI
DSI1_D2N_T0B	R31	AIO	DSI interface	AVDD12_DSI
DSI1_D2P_T0A	T31	AIO	DSI interface	AVDD12_DSI
DSI1_D3N	N34	AIO	DSI interface	AVDD12_DSI
DSI1_D3P_T2C	N35	AIO	DSI interface	AVDD12_DSI
CSI0A_L0N_T0B	AJ2	AIO	CSI interface	AVDD12_CSI
CSI0A_L0P_T0A	AJ1	AIO	CSI interface	AVDD12_CSI
CSI0A_L1N_T1A	AK3	AIO	CSI interface	AVDD12_CSI
CSI0A_L1P_T0C	AK4	AIO	CSI interface	AVDD12_CSI
CSI0A_L2N_T1C	AK1	AIO	CSI interface	AVDD12_CSI
CSI0A_L2P_T1B	AK2	AIO	CSI interface	AVDD12_CSI
CSI0B_L0N_T0B	AL2	AIO	CSI interface	AVDD12_CSI
CSI0B_L0P_T0A	AL1	AIO	CSI interface	AVDD12_CSI
CSI0B_L1N_T1A	AM4	AIO	CSI interface	AVDD12_CSI
CSI0B_L1P_T0C	AL4	AIO	CSI interface	AVDD12_CSI
CSI0B_L2N_T1C	AM1	AIO	CSI interface	AVDD12_CSI
CSI0B_L2P_T1B	AM2	AIO	CSI interface	AVDD12_CSI

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Pin name	Pin no.	Type	Description	Power domain
CSI1A_L0N_T0B	AF1	AIO	CSI interface	AVDD12_CSI
CSI1A_L0P_T0A	AF2	AIO	CSI interface	AVDD12_CSI
CSI1A_L1N_T1A	AF4	AIO	CSI interface	AVDD12_CSI
CSI1A_L1P_T0C	AF3	AIO	CSI interface	AVDD12_CSI
CSI1A_L2N_T1C	AG1	AIO	CSI interface	AVDD12_CSI
CSI1A_L2P_T1B	AG2	AIO	CSI interface	AVDD12_CSI
CSI1B_L0N_T0B	AG5	AIO	CSI interface	AVDD12_CSI
CSI1B_L0P_T0A	AG4	AIO	CSI interface	AVDD12_CSI
CSI1B_L1N_T1A	AH2	AIO	CSI interface	AVDD12_CSI
CSI1B_L1P_T0C	AH1	AIO	CSI interface	AVDD12_CSI
CSI1B_L2N_T1C	AJ4	AIO	CSI interface	AVDD12_CSI
CSI1B_L2P_T1B	AH4	AIO	CSI interface	AVDD12_CSI
CSI2A_L0N_T0B	AC4	AIO	CSI interface	AVDD12_CSI
CSI2A_L0P_T0A	AC5	AIO	CSI interface	AVDD12_CSI
CSI2A_L1N_T1A	AC2	AIO	CSI interface	AVDD12_CSI
CSI2A_L1P_T0C	AC3	AIO	CSI interface	AVDD12_CSI
CSI2A_L2N_T1C	AD2	AIO	CSI interface	AVDD12_CSI
CSI2A_L2P_T1B	AD3	AIO	CSI interface	AVDD12_CSI
CSI2B_L0N_T0B	AD4	AIO	CSI interface	AVDD12_CSI
CSI2B_L0P_T0A	AD5	AIO	CSI interface	AVDD12_CSI
CSI2B_L1N_T1A	AE1	AIO	CSI interface	AVDD12_CSI
CSI2B_L1P_T0C	AE2	AIO	CSI interface	AVDD12_CSI
CSI2B_L2N_T1C	AE4	AIO	CSI interface	AVDD12_CSI
CSI2B_L2P_T1B	AE5	AIO	CSI interface	AVDD12_CSI
CSI3A_L0N_T0B	W2	AIO	CSI interface	AVDD12_CSI
CSI3A_L0P_T0A	W1	AIO	CSI interface	AVDD12_CSI
CSI3A_L1N_T1A	Y1	AIO	CSI interface	AVDD12_CSI
CSI3A_L1P_T0C	Y2	AIO	CSI interface	AVDD12_CSI
CSI3A_L2N_T1C	AA4	AIO	CSI interface	AVDD12_CSI
CSI3A_L2P_T1B	Y3	AIO	CSI interface	AVDD12_CSI
CSI3B_L0N_T0B	AB3	AIO	CSI interface	AVDD12_CSI
CSI3B_L0P_T0A	AB4	AIO	CSI interface	AVDD12_CSI
CSI3B_L1N_T1A	AA1	AIO	CSI interface	AVDD12_CSI
CSI3B_L1P_T0C	AA2	AIO	CSI interface	AVDD12_CSI
CSI3B_L2N_T1C	AB1	AIO	CSI interface	AVDD12_CSI
CSI3B_L2P_T1B	AB2	AIO	CSI interface	AVDD12_CSI
SSUSB				
SSUSB_RXN	V32	AIO	SSUSB RXDATA	AVDD12_SSUSB
SSUSB_RXP	V31	AIO	SSUSB RXDATA	AVDD12_SSUSB
SSUSB_TXN	U35	AIO	SSUSB TXDATA	AVDD12_SSUSB
SSUSB_TXP	U34	AIO	SSUSB TXDATA	AVDD12_SSUSB
DPTX				

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Pin name	Pin no.	Type	Description	Power domain
DP_LN0_TXN	AA30	AIO	DPTX interfcae	AVDD18_DPTX
DP_LN0_TXP	Y30	AIO	DPTX interfcae	AVDD18_DPTX
DP_LN1_TXN	AA35	AIO	DPTX interfcae	AVDD18_DPTX
DP_LN1_TXP	AA34	AIO	DPTX interfcae	AVDD18_DPTX
DPAUXN	AB33	AIO	DPTX interfcae	AVDD18_DPTX
DPAUXP	AB32	AIO	DPTX interfcae	AVDD18_DPTX
WBG				
XIN_WBG	G5	AIO	WBG crystal clock input	AVDD18_WBG
WF0_IN	A5	AIO	Wi-Fi I channel 0 negative-end	AVDD18_WBG
WF0_IP	B5	AIO	Wi-Fi I channel 0 positive-end	AVDD18_WBG
WF0_QN	C4	AIO	Wi-Fi Q channel 0 negative-end	AVDD18_WBG
WF0_QP	D4	AIO	Wi-Fi Q channel 0 positive-end	AVDD18_WBG
WF1_IN	A7	AIO	Wi-Fi I channel 1 negative-end	AVDD18_WBG
WF1_IP	B7	AIO	Wi-Fi I channel 1 positive-end	AVDD18_WBG
WF1_QN	D6	AIO	Wi-Fi Q channel 1 negative-end	AVDD18_WBG
WF1_QP	C6	AIO	Wi-Fi Q channel 1 positive-end	AVDD18_WBG
BT_IN	D3	AIO	BT I channel negative-end	AVDD18_WBG
BT_IP	C3	AIO	BT I channel positive-end	AVDD18_WBG
BT_QN	E2	AIO	BT Q channel negative-end	AVDD18_WBG
BT_QP	E3	AIO	BT Q channel positive-end	AVDD18_WBG
GPS_Q_L5	G3	AIO	GPS L5 Q channel	AVDD18_WBG
GPS_I_L5	G2	AIO	GPS L5 I channel	AVDD18_WBG
GPS_Q_L1	F2	AIO	GPS L1 Q channel	AVDD18_WBG
GPS_I_L1	F1	AIO	GPS L1 I channel	AVDD18_WBG
USB				
USB_DM	W34	AIO	USB D+ differential data line	AVDD33_USB
USB_DP	W33	AIO	USB D- differential data line	AVDD33_USB
UFS				
UFS_PLL_CKREF	E14	AIO	26 MHz clock input for UFS	AVDD18_UFS
UFS_REFCK_OUT	E16	AIO	UFS interface	AVDD18_UFS
UFS_TX0P	C15	AIO	UFS interface	AVDD18_UFS
UFS_TX0N	D15	AIO	UFS interface	AVDD18_UFS
UFS_TX1P	C13	AIO	UFS interface	AVDD18_UFS
UFS_TX1N	B13	AIO	UFS interface	AVDD18_UFS
UFS_RX0P	B17	AIO	UFS interface	AVDD18_UFS
UFS_RX0N	B18	AIO	UFS interface	AVDD18_UFS
UFS_RX1P	D17	AIO	UFS interface	AVDD18_UFS
UFS_RX1N	D18	AIO	UFS interface	AVDD18_UFS
UFS_RST_N	A17	AIO	UFS interface	AVDD18_UFS
AUXADC				
AUXIN0	Y32	AIO	AUXADC ch 0	AVDD18_USB
AUXIN1	Y33	AIO	AUXADC ch 1	AVDD18_USB

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Pin name	Pin no.	Type	Description	Power domain
AUXIN2	W31	AIO	AUXADC ch 2	AVDD18_USB
AUXIN3	V34	AIO	AUXADC ch 3	AVDD18_USB
AUXIN4	V33	AIO	AUXADC ch 4	AVDD18_USB
AUXIN5	W32	AIO	AUXADC ch 5	AVDD18_USB
General purpose				
PERIPHERAL_EN0	AM9	DIO	PERIPHERAL_EN0	DVDD18
PERIPHERAL_EN1	AP9	DIO	PERIPHERAL_EN1	DVDD18
PERIPHERAL_EN2	AN9	DIO	PERIPHERAL_EN2	DVDD18
PERIPHERAL_EN3	AN10	DIO	PERIPHERAL_EN3	DVDD18
PERIPHERAL_EN4	B33	DIO	PERIPHERAL_EN4	DVDD18
PERIPHERAL_EN5	C33	DIO	PERIPHERAL_EN5	DVDD18
PERIPHERAL_EN6	C34	DIO	PERIPHERAL_EN6	DVDD18
PERIPHERAL_EN7	C32	DIO	PERIPHERAL_EN7	DVDD18
PERIPHERAL_EN8	D31	DIO	PERIPHERAL_EN8	DVDD18
MISC				
TN_APPLLGP	R17	AIO	Reserved	
TP_APPLLGP	P17	AIO	Reserved	
Analog power				
AVDD12_APPLLGP	T17	P	Analog power for APPLL	AVDD12_APPLLGP
AVDD12_CKBUF_UFS	B15	P	Analog power for UFS	AVDD12_CKBUF_UFS
AVDD12_CKSQ	K32	P	Analog power for CKSQ	AVDD12_CKSQ
AVDD12_CSI	AN2	P	Analog power for CSI	AVDD12_CSI
AVDD12_DPTX	Y35	P	Analog power for DPTX	AVDD12_DPTX
AVDD12_DRF	AH35	P	Analog power for modem	AVDD12_DRF
AVDD12_DSI	R35	P	Analog power for DSI	AVDD12_DSI
AVDD12_MDPLLGP	AK21	P	Analog power for modem PLL	AVDD12_MDPLLGP
AVDD12_SSUSB	T35	P	Analog power for SSUSB	AVDD12_SSUSB
AVDD12_UFS	B15	P	Analog power for UFS	AVDD12_UFS
AVDD12_USB	T34	P	Analog power input USB	AVDD12_USB
AVDD12_WBG	F5	P	Analog power for WBG (Wi-Fi, BT, GPS)	AVDD12_WBG
AVDD18_APPLLGP	U17	P	Analog power input 1.8V for APPLL	AVDD18_APPLLGP
AVDD18_CKSQ	K33	P	Analog power input 1.8V for CKSQ	AVDD18_CKSQ
AVDD18_DPTX	AB34	P	Analog power input 1.8V for DPTX	AVDD18_DPTX
AVDD18_DRF	AJ35	P	Analog power input 1.8V for modem	AVDD18_DRF
AVDD18_GPU	AA10	P	Analog power 1.8V for GPU	AVDD18_GPU
AVDD18_MDPLLGP	AK22	P	Analog power 1.8V for modem PLL	AVDD18_MDPLLGP
AVDD18_PROC	K25	P	Analog power 1.8V for CPU	AVDD18_PROC
AVDD18_UFS	C8	P	Analog power 1.8V for UFS	AVDD18_UFS
AVDD18_USB	U32	P	Analog power 1.8V for USB	AVDD18_USB
AVDD18_WBG	E5	P	Analog power 1.8V for WBG (Wi-Fi, BT, GPS)	AVDD18_WBG
AVDD33_USB	V35	P	Analog power 3.3V for USB	AVDD33_USB

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Pin name	Pin no.	Type	Description	Power domain
VDD1_EMI_B	AN1…	DIO	DRAM power	VDD1_EMI
VDD1_EMI_T	A14…	DIO	DRAM power	VDD1_EMI
VDD2_EMI_B	AN3…	DIO	DRAM power	VDD2_EMI
VDD2_EMI_T	A16…	DIO	DRAM power	VDD2_EMI
VDDQ_EMI_B	AP2…	DIO	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A15…	DIO	DRAM power	VDDQ_EMI
AVDD075_EMI0	F7…	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI1	AK6…	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI2	F28…	DIO	DRAM power	AVDD075_EMI
AVDD075_EMI3	AK26…	DIO	DRAM power	AVDD075_EMI
AVDD12_EMI0	F11…	DIO	DRAM power	AVDD12_EMI
AVDD12_EMI1	AK10…	DIO	DRAM power	AVDD12_EMI
AVDD12_EMI2	F26…	DIO	DRAM power	AVDD12_EMI
AVDD12_EMI3	AK24…	DIO	DRAM power	AVDD12_EMI
AVDDQ_EMI0	F6…	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI1	AK5…	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI2	F27…	DIO	DRAM power	AVDDQ_EMI
AVDDQ_EMI3	AK25…	DIO	DRAM power	AVDDQ_EMI
Digital power				
DVDD_ADSP	F15…	P	Digital power input for ADSP	-
DVDD_APU	M25…	P	Digital power input for APU	-
DVDD_CORE	G9…	P	Digital power input for Vcore	-
DVDD_DLA	H25…	P	Digital power input for MDLA	-
DVDD_GPU	V5…	P	Digital power input for GPU	-
DVDD_MODEM	V22…	P	Digital power input for modem	-
DVDD_NR	V26…	P	Digital power input for NR	-
DVDD_PROC_B	F18…	P	Digital power input for Big Core	-
DVDD_PROC_L	K19…	P	Digital power input for Little Core	
DVDD_SRAM_APU	N30…	P	Digital power input for APU SRAM	
DVDD_SRAM_CORE	J7…	P	Digital power input for Core SRAM	-
DVDD_SRAM_GPU	V7…	P	Digital power input for GPU SRAM	-
DVDD_SRAM_MODEM	AB31…	P	Digital power input for modem SRAM	-
DVDD_SRAM_NR	L18	P	Digital power input for NR SRAM	-
DVDD_SRAM_PROC_B	M24	P	Digital power input for Big Core SRAM	-
DVDD_SRAM_PROC_L	AL15	P	Digital power input for Little Core SRAM	-
DVDD18_IOBM	AN33	P	Digital power input for I/O	-
DVDD18_IOLB	F35	P	Digital power input for I/O	
DVDD18_IOLT	W3	P	Digital power input for I/O	-
DVDD18_IORM	K1	P	Digital power input for I/O	
DVDD18_IORT	E25	P	Digital power input for I/O	-
DVDD18_IOTM	B16	P	Digital power input for I/O	-
DVDD18_MSDC0	C8	P	Digital power input for MSDC0	

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Pin name	Pin no.	Type	Description	Power domain
DVDD18_MSDC1	Y4	P	Digital power input for MSDC1	
DVDD18_MSDC2	J32	P	Digital power input for MSDC2	
DVDD18_SIM1	H31	P	Digital power input for SIM1	
DVDD18_SIM2	AB5	P	Digital power input for SIM2	
DVDD18_VQPS	AB35	P	Digital power input for VQPS	
DVDD28_MSDC1	V1	P	Digital power input for MSDC1	
DVDD28_MSDC2	K35	P	Digital power input for MSDC2	
DVDD28_SIM1	K34	P	Digital power input for SIM1	
DVDD28_SIM2	F17…	P	Digital power input for SIM2	
ESD				
CDM1P5A	AR6	G	Reserved	-
CDM3P0A	AP6	G	Reserved	-
Digital ground				
DVSS	A4, …	G		-

Table 2-5. Detailed TOP ball pin description

Pin name	Pin no.	Type	Description	Power domain
EMI				
EMI0_CA0	B6	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA1	D6	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA2	E8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA3	B9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA4	D9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA5	E9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_C	C8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_T	B8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE0	D7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE1	E7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS0	A7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS1	B7	DIO	DRAM interface	AVDDQ_EMI
EMI0_DMI0	E3	DIO	DRAM interface	AVDDQ_EMI
EMI0_DMI1	E12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ0	C1	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ1	E1	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ10	D13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ11	B13	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ12	D11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ13	B11	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ14	E10	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ15	C10	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ2	B2	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ3	D2	DIO	DRAM interface	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
EMI0_DQ4	B4	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ5	D4	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ6	C5	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ7	E5	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ8	E14	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQ9	C14	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS0_C	C3	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS0_T	B3	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS1_C	C12	DIO	DRAM interface	AVDDQ_EMI
EMI0_DQS1_T	B12	DIO	DRAM interface	AVDDQ_EMI
EMI0_RESET_N	C15	DIO	DRAM interface	AVDDQ_EMI
EMI0_ZQ0	E15	DIO	DRAM interface	AVDDQ_EMI
EMI0_ZQ1	D15	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA0	AH6	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA1	AF6	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA2	AE8	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA3	AH9	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA4	AF9	DIO	DRAM interface	AVDDQ_EMI
EMI1_CA5	AE9	DIO	DRAM interface	AVDDQ_EMI
EMI1_CK_C	AG8	DIO	DRAM interface	AVDDQ_EMI
EMI1_CK_T	AH8	DIO	DRAM interface	AVDDQ_EMI
EMI1_CKE0	AF7	DIO	DRAM interface	AVDDQ_EMI
EMI1_CKE1	AE7	DIO	DRAM interface	AVDDQ_EMI
EMI1_CS0	AJ7	DIO	DRAM interface	AVDDQ_EMI
EMI1_CS1	AH7	DIO	DRAM interface	AVDDQ_EMI
EMI1_DMI0	AE3	DIO	DRAM interface	AVDDQ_EMI
EMI1_DMI1	AE12	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ0	AG1	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ1	AE1	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ10	AF13	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ11	AH13	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ12	AF11	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ13	AH11	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ14	AE10	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ15	AG10	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ2	AH2	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ3	AF2	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ4	AH4	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ5	AF4	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ6	AG5	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ7	AE5	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ8	AE14	DIO	DRAM interface	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
EMI1_DQ9	AG14	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS0_C	AG3	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS0_T	AH3	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS1_C	AG12	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQS1_T	AH12	DIO	DRAM interface	AVDDQ_EMI
EMI2_CA0	B24	DIO	DRAM interface	AVDDQ_EMI
EMI2_CA1	D24	DIO	DRAM interface	AVDDQ_EMI
EMI2_CA2	E22	DIO	DRAM interface	AVDDQ_EMI
EMI2_CA3	B21	DIO	DRAM interface	AVDDQ_EMI
EMI2_CA4	D21	DIO	DRAM interface	AVDDQ_EMI
EMI2_CA5	E21	DIO	DRAM interface	AVDDQ_EMI
EMI2_CK_C	C22	DIO	DRAM interface	AVDDQ_EMI
EMI2_CK_T	B22	DIO	DRAM interface	AVDDQ_EMI
EMI2_CKE0	D23	DIO	DRAM interface	AVDDQ_EMI
EMI2_CKE1	E23	DIO	DRAM interface	AVDDQ_EMI
EMI2_CS0	A23	DIO	DRAM interface	AVDDQ_EMI
EMI2_CS1	B23	DIO	DRAM interface	AVDDQ_EMI
EMI2_DMI0	E27	DIO	DRAM interface	AVDDQ_EMI
EMI2_DMI1	E18	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ0	C29	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ1	E29	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ10	D17	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ11	B17	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ12	D19	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ13	B19	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ14	E20	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ15	C20	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ2	B28	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ3	D28	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ4	B26	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ5	D26	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ6	C25	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ7	E25	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ8	E16	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQ9	C16	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQS0_C	C27	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQS0_T	B27	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQS1_C	C18	DIO	DRAM interface	AVDDQ_EMI
EMI2_DQS1_T	B18	DIO	DRAM interface	AVDDQ_EMI
EMI3_CA0	AH24	DIO	DRAM interface	AVDDQ_EMI
EMI3_CA1	AF24	DIO	DRAM interface	AVDDQ_EMI
EMI3_CA2	AE22	DIO	DRAM interface	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
EMI3_CA3	AH21	DIO	DRAM interface	AVDDQ_EMI
EMI3_CA4	AF21	DIO	DRAM interface	AVDDQ_EMI
EMI3_CA5	AE21	DIO	DRAM interface	AVDDQ_EMI
EMI3_CK_C	AG22	DIO	DRAM interface	AVDDQ_EMI
EMI3_CK_T	AH22	DIO	DRAM interface	AVDDQ_EMI
EMI3_CKE0	AF23	DIO	DRAM interface	AVDDQ_EMI
EMI3_CKE1	AE23	DIO	DRAM interface	AVDDQ_EMI
EMI3_CS0	AJ23	DIO	DRAM interface	AVDDQ_EMI
EMI3_CS1	AH23	DIO	DRAM interface	AVDDQ_EMI
EMI3_DMI0	AE27	DIO	DRAM interface	AVDDQ_EMI
EMI3_DMI1	AE18	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ0	AG29	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ1	AE29	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ10	AF17	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ11	AH17	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ12	AF19	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ13	AH19	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ14	AE20	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ15	AG20	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ2	AH28	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ3	AF28	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ4	AH26	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ5	AF26	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ6	AG25	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ7	AE25	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ8	AE16	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQ9	AG16	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQS0_C	AG27	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQS0_T	AH27	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQS1_C	AG18	DIO	DRAM interface	AVDDQ_EMI
EMI3_DQS1_T	AH18	DIO	DRAM interface	AVDDQ_EMI
EMI3_ZQ0	AE15	DIO	DRAM interface	AVDDQ_EMI
EMI3_ZQ1	AF15	DIO	DRAM interface	AVDDQ_EMI
VDD1_EMI_B	AH1	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AH10	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AH14	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AH16	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AH20	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AH29	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AJ5	P	DRAM power	VDD1_EMI
VDD1_EMI_B	AJ25	P	DRAM power	VDD1_EMI
VDD1_EMI_T	A5	P	DRAM power	VDD1_EMI

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Pin name	Pin no.	Type	Description	Power domain
VDD1_EMI_T	A25	P	DRAM power	VDD1_EMI
VDD1_EMI_T	B1	P	DRAM power	VDD1_EMI
VDD1_EMI_T	B10	P	DRAM power	VDD1_EMI
VDD1_EMI_T	B14	P	DRAM power	VDD1_EMI
VDD1_EMI_T	B16	P	DRAM power	VDD1_EMI
VDD1_EMI_T	B20	P	DRAM power	VDD1_EMI
VDD1_EMI_T	B29	P	DRAM power	VDD1_EMI
VDD2_EMI_B	AD1	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AD2	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AD28	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AD29	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AE6	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AE24	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AG7	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AG9	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AG21	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AG23	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ2	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ6	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ8	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ10	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ14	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ16	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ20	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ22	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ24	P	DRAM power	VDD2_EMI
VDD2_EMI_B	AJ28	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A2	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A6	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A8	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A10	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A14	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A16	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A20	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A22	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A24	P	DRAM power	VDD2_EMI
VDD2_EMI_T	A28	P	DRAM power	VDD2_EMI
VDD2_EMI_T	C7	P	DRAM power	VDD2_EMI
VDD2_EMI_T	C9	P	DRAM power	VDD2_EMI
VDD2_EMI_T	C21	P	DRAM power	VDD2_EMI
VDD2_EMI_T	C23	P	DRAM power	VDD2_EMI
VDD2_EMI_T	E6	P	DRAM power	VDD2_EMI

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Pin name	Pin no.	Type	Description	Power domain
VDD2_EMI_T	E24	P	DRAM power	VDD2_EMI
VDD2_EMI_T	F1	P	DRAM power	VDD2_EMI
VDD2_EMI_T	F2	P	DRAM power	VDD2_EMI
VDD2_EMI_T	F28	P	DRAM power	VDD2_EMI
VDD2_EMI_T	F29	P	DRAM power	VDD2_EMI
VDDQ_EMI_B	AF1	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF3	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF5	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF10	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF12	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF14	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF16	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF18	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF20	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF25	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF27	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AF29	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AJ4	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AJ11	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AJ13	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AJ17	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AJ19	P	DRAM power	VDDQ_EMI
VDDQ_EMI_B	AJ26	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A4	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A11	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A13	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A17	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A19	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A26	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D1	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D3	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D5	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D10	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D12	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D14	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D16	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D18	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D20	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D25	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D27	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	D29	P	DRAM power	VDDQ_EMI
VDDQ_EMI_T	A11	P	DRAM power	VDDQ_EMI

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Table 2-6. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 2-7. Absolute maximum ratings for power supply

Symbol or pin name	Description	Max.	Unit
AVDD04_DSI	Analog power	0.88	V
AVDD12_APPLLGP	Analog power	1.32	V
AVDD12_CKBUF_UFS	Analog power	1.32	V
AVDD12_CKSQ	Analog power	1.32	V
AVDD12_CSI	Analog power	1.32	V
AVDD12_DPTX	Analog power	1.32	V
AVDD12_DRF	Analog power	1.32	V
AVDD12_DSI	Analog power	1.32	V
AVDD12_MDPLLGP	Analog power	1.32	V
AVDD12_SSUSB	Analog power	1.32	V
AVDD12_UFS	Analog power	1.32	V
AVDD12_USB	Analog power	1.32	V
AVDD12_WBG	Analog power	1.32	V
AVDD18_APPLLGP	Analog power	1.98	V
AVDD18_CKSQ	Analog power	1.98	V
AVDD18_DPTX	Analog power	1.98	V
AVDD18_DRF	Analog power	1.98	V
AVDD18_GPU	Analog power	1.98	V
AVDD18_MDPLLGP	Analog power	1.98	V
AVDD18_PROC	Analog power	1.98	V
AVDD18_UFS	Analog power	1.98	V
AVDD18_USB	Analog power	1.98	V
AVDD18_WBG	Analog power	1.98	V
AVDD33_USB	Analog power	3.22	V
AVDDQ_EMI0/1/2/3	Analog power	0.63	V
AVDD075_EMI0/1/2/3	Analog power	0.825	V
AVDD12_EMI0/1/2/3	Analog power	1.26	V
AVDD18_EMI0/1/2/3	Analog power	1.98	V
DVDD18_IOBM DVDD18_IOLB DVDD18_IOLT DVDD18_IORM DVDD18_IORT DVDD18_TM DVDD18_SIM1 DVDD18_SIM2	Digital power input for 1.8V I/O	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1. 95	V
DVDD18_MSDC1	Digital power input for MSDC1	1. 95	V
DVDD28_MSDC1	Digital power input for MSDC1	3.15	V

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Symbol or pin name	Description	Max.	Unit
DVDD18_MSDC2	Digital power input for MSDC2	1. 95	V
DVDD28_MSDC2	Digital power input for MSDC2	3.15	V
DVDD28_SIM1	Digital power input for SIM1	3.15	V
DVDD28_SIM2	Digital power input for SIM2	3.15	V
DVDD_CORE	Digital power input for CORE	0.810	V
DVDD_GPU	Digital power input for GPU	0.864	V
DVDD_PROC_B	Digital power input for Big Core	1.051	V
DVDD_PROC_L	Digital power input for Little Core	1.0	V
DVDD_APU	Digital power input for VPU	0.891	V
DVDD_DLA	Digital power input for MDLA	0.891	V
DVDD_ADSP	Digital power input for ADSP	0.810	V
DVDD_NR	Digital power input for NR	0.864	V
DVDD_MODEM	Digital power input for modem	0.864	V
DVDD_SRAM_CORE	Digital power input for Vcore SRAM	0.810	V
DVDD_SRAM_GPU	Digital power input for GPU SRAM	0.864	V
DVDD_SRAM_MODEM	Digital power input for modem SRAM	0.864	V
DVDD_SRAM_NR	Digital power input for NR SRAM	0.864	V
DVDD_SRAM_APU	Digital power input for APU SRAM	0.891	V
DVDD_SRAM_PROC_B	Digital power input for Big Core SRAM	1.051	V
DVDD_SRAM_PROC_L	Digital power input for Little Core SRAM	1.0	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-8. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD04_DSI	Analog power	0.7125	0.75	0.84	V
AVDD12_APPLLGP	Analog power	1.14	1.2	1.26	V
AVDD12_CKBUF_UFS	Analog power	1.14	1.2	1.26	V
AVDD12_CKSQ	Analog power	1.14	1.2	1.26	V
AVDD12_CSI	Analog power	1.14	1.2	1.26	V
AVDD12_DPTX	Analog power	1.14	1.2	1.26	V
AVDD12_DRF	Analog power	1.14	1.2	1.26	V
AVDD12_DSI	Analog power	1.14	1.2	1.26	V
AVDD12_MDPLLGP	Analog power	1.14	1.2	1.26	V
AVDD12_SSUSB	Analog power	1.14	1.2	1.26	V
AVDD12_UFS	Analog power	1.14	1.2	1.26	V
AVDD12_USB	Analog power	1.14	1.2	1.26	V
AVDD12_WBG	Analog power	1.14	1.2	1.26	V
AVDD18_APPLLGP	Analog power	1.71	1.8	1.89	V
AVDD18_CKSQ	Analog power	1.71	1.8	1.89	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_DPTX	Analog power	1.71	1.8	1.89	V
AVDD18_DRF	Analog power	1.71	1.8	1.89	V
AVDD18_GPU	Analog power	1.71	1.8	1.89	V
AVDD18_MDPLLGP	Analog power	1.71	1.8	1.89	V
AVDD18_PROC	Analog power	1.71	1.8	1.89	V
AVDD18_UFS	Analog power	1.71	1.8	1.89	V
AVDD18_USB	Analog power	1.71	1.8	1.89	V
AVDD18_WBG	Analog power	1.71	1.8	1.89	V
AVDD33_USB	Analog power	2.92	3.07	3.22	V
AVDDQ_EMI0/1/2/3	Analog power	0.57	0.6	0.63	V
AVDD075_EMI0/1/2/3	Analog power	0.675	0.75	0.825	V
AVDD12_EMI0/1/2/3	Analog power	1.14	1.2	1.26	V
AVDD18_EMI0/1/2/3	Analog power	1.62	1.8	1.98	V
DVDD18_IOBM DVDD18_IOLB DVDD18_IOLT DVDD18_IORM DVDD18_IORT DVDD18_TM DVDD18_SIM1 DVDD18_SIM2	Digital power input for 1.8V I/O	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.70	1.8	1.95	V
DVDD18_MSDC1	Digital power input for MSDC1	1.70	1.8	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	2.70	3	3.15	V
DVDD18_MSDC2	Digital power input for MSDC2	1.70	1.8	1.95	V
DVDD28_MSDC2	Digital power input for MSDC2	2.70	3	3.15	V
DVDD28_SIM1	Digital power input for SIM1	2.70	3	3.15	V
DVDD28_SIM2	Digital power input for SIM2	2.70	3	3.15	V
DVDD_CORE	Digital power input for CORE	0.703	0.75	0.810	V
		0.680	0.725	0.783	V
		0.609	0.65	0.702	V
		0.563	0.6	0.648	V
		0.539	0.575	0.621	V
		0.516	0.55	0.594	V
DVDD_GPU	Digital power input for GPU	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.516	0.55	0.594	V
DVDD_PROC_B	Digital power input for Big Core	0.912	0.973	1.051	V
		0.844	0.9	0.972	V
		0.750	0.8	0.864	V
		0.656	0.7	0.756	V
		0.563	0.6	0.648	V
		0.516	0.55	0.594	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD_PROC_L	Digital power input for Little Core	0.868	0.926	1.0	V
		0.750	0.8	0.864	V
		0.656	0.7	0.756	V
		0.563	0.6	0.648	V
		0.516	0.55	0.594	V
DVDD_APU	Digital power input for VPU	0.773	0.825	0.891	V
		0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.539	0.575	0.621	V
DVDD_MDLA	Digital power input for MDLA	0.773	0.825	0.891	V
		0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.539	0.575	0.621	V
DVDD_MODEM	Digital power input for modem	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.656	0.7	0.756	V
		0.609	0.65	0.702	V
		0.563	0.6	0.648	V
DVDD_NR	Digital power input for NR	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.656	0.7	0.756	V
		0.609	0.65	0.702	V
		0.563	0.6	0.648	V
DVDD_ADSP	Digital power input for ADSP	0.703	0.75	0.810	V
DVDD_SRAM_CORE	Digital power input for Vcore SRAM	0.703	0.75	0.810	V
DVDD_SRAM_APU	Digital power input for APU SRAM	0.773	0.825	0.891	V
		0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_GPU	Digital power input for GPU SRAM	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_MODEM	Digital power input for modem SRAM	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_NR	Digital power input for NR SRAM	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_PROC_B	Digital power input for Big Core SRAM	0.912	0.973	1.051	V
		0.844	0.9	0.972	V
		0.750	0.8	0.864	V
DVDD_SRAM_PROC_L	Digital power input for Little Core SRAM	0.868	0.926	1.0	V

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).

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2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices will require baking before being mounted if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-9. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD04_DSI	Analog power	0.7125	0.75	0.84	V
AVDD12_APPLLGP	Analog power	1.14	1.2	1.26	V
AVDD12_CKBUF_UFS	Analog power	1.14	1.2	1.26	V
AVDD12_CKSQ	Analog power	1.14	1.2	1.26	V
AVDD12_CSI	Analog power	1.14	1.2	1.26	V
AVDD12_DPTX	Analog power	1.14	1.2	1.26	V
AVDD12_DRF	Analog power	1.14	1.2	1.26	V
AVDD12_DSI	Analog power	1.14	1.2	1.26	V
AVDD12_MDPLLGP	Analog power	1.14	1.2	1.26	V
AVDD12_SSUSB	Analog power	1.14	1.2	1.26	V
AVDD12_UFS	Analog power	1.14	1.2	1.26	V
AVDD12_USB	Analog power	1.14	1.2	1.26	V
AVDD12_WBG	Analog power	1.14	1.2	1.26	V
AVDD18_APPLLGP	Analog power	1.71	1.8	1.89	V
AVDD18_CKSQ	Analog power	1.71	1.8	1.89	V
AVDD18_DPTX	Analog power	1.71	1.8	1.89	V
AVDD18_DRF	Analog power	1.71	1.8	1.89	V
AVDD18_GPU	Analog power	1.71	1.8	1.89	V
AVDD18_MDPLLGP	Analog power	1.71	1.8	1.89	V
AVDD18_PROC	Analog power	1.71	1.8	1.89	V
AVDD18_UFS	Analog power	1.71	1.8	1.89	V
AVDD18_USB	Analog power	1.71	1.8	1.89	V
AVDD18_WBG	Analog power	1.71	1.8	1.89	V
AVDD33_USB	Analog power	2.92	3.07	3.22	V
AVDDQ_EMI0/1/2/3	Analog power	0.57	0.6	0.63	V
AVDD075_EMI0/1/2/3	Analog power	0.675	0.75	0.825	V
AVDD12_EMI0/1/2/3	Analog power	1.14	1.2	1.26	V
AVDD18_EMI0/1/2/3	Analog power	1.62	1.8	1.98	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18_IOBM DVDD18_IOLB DVDD18_IOLT DVDD18_IORM DVDD18_IORT DVDD18_TM DVDD18_SIM1 DVDD18_SIM2	Digital power input for 1.8V I/O	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.70	1.8	1.95	V
DVDD18_MSDC1	Digital power input for MSDC1	1.70	1.8	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	2.70	3	3.15	V
DVDD18_MSDC2	Digital power input for MSDC2	1.70	1.8	1.95	V
DVDD28_MSDC2	Digital power input for MSDC2	2.70	3	3.15	V
DVDD28_SIM1	Digital power input for SIM1	2.70	3	3.15	V
DVDD28_SIM2	Digital power input for SIM2	2.70	3	3.15	V
DVDD_CORE	Digital power input for CORE	0.703	0.75	0.810	V
		0.680	0.725	0.783	V
		0.609	0.65	0.702	V
		0.563	0.6	0.648	V
		0.539	0.575	0.621	V
		0.516	0.55	0.594	V
DVDD_GPU	Digital power input for GPU	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.516	0.55	0.594	V
DVDD_PROC_B	Digital power input for Big Core	0.912	0.973	1.051	V
		0.844	0.9	0.972	V
		0.750	0.8	0.864	V
		0.656	0.7	0.756	V
		0.563	0.6	0.648	V
		0.516	0.55	0.594	V
DVDD_PROC_L	Digital power input for Little Core	0.868	0.926	1.0	V
		0.750	0.8	0.864	V
		0.656	0.7	0.756	V
		0.563	0.6	0.648	V
		0.516	0.55	0.594	V
DVDD_APU	Digital power input for VPU	0.773	0.825	0.891	V
		0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.539	0.575	0.621	V
DVDD_MDLA	Digital power input for MDLA	0.773	0.825	0.891	V
		0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.539	0.575	0.621	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD_MODEM	Digital power input for modem	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.656	0.7	0.756	V
		0.609	0.65	0.702	V
		0.563	0.6	0.648	V
DVDD_NR	Digital power input for NR	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
		0.656	0.7	0.756	V
		0.609	0.65	0.702	V
		0.563	0.6	0.648	V
DVDD_ADSP	Digital power input for ADSP	0.703	0.75	0.810	V
DVDD_SRAM_CORE	Digital power input for Vcore SRAM	0.703	0.75	0.810	V
DVDD_SRAM_APU	Digital power input for APU SRAM	0.773	0.825	0.891	V
		0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_GPU	Digital power input for GPU SRAM	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_MODEM	Digital power input for modem SRAM	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_NR	Digital power input for NR SRAM	0.750	0.8	0.864	V
		0.703	0.75	0.810	V
DVDD_SRAM_PROC_B	Digital power input for Big Core SRAM	0.912	0.973	1.051	V
		0.844	0.9	0.972	V
		0.750	0.8	0.864	V
DVDD_SRAM_PROC_L	Digital power input for Little Core SRAM	0.868	0.926	1.0	V

Table 2-10. RTC DC electrical characteristics (DVDD18_IOLT = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
F_{RTC}	Input clock frequency		32		kHz
DC_{RTC}	Input signal duty cycle	45	50	55	%

2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-11. SPI, I2S DC electrical characteristics (DVDD18_IORB = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V

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Parameter	Description	Min.	Typ.	Max.	Unit
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

2.2.4.3 I2C/I3C DC Electrical Characteristics

Table 2-12. I2C/I3C DC electrical characteristics (DVDD18_IORB = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-13. I2C3 DC electrical characteristics (DVDD18_IOLB = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-14. MSDC0 DC electrical characteristics (DVDD28_MSDC0 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD28_MSDC0		DVDD28_MSDC0 + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD28_MSDC0	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-15. MSDC1 DC electrical characteristics (DVDD28_MSDC1 = 2.8V/3.0V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.75*DVDD28_MSDC1		DVDD28_MSDC1 + 0.15	V
VIL	Input logic high voltage	-0.3		0.25*DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.625*DVDD28_MSDC1		DVDD28_MSDC1 + 0.15	V
VOL	DC output logic high voltage	-0.3		0.125*DVDD28_MSDC1	V

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Table 2-16. MSDC1 DC electrical characteristics (DVDD28_MSDC1 = 1.8V)

Parameter	Description	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.7*DVDD28_MSDC1		DVDD28_MSDC1 + 0.15	V
VIL	Input logic high voltage	-0.3		0.3*DVDD28_MSDC1	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.15	V
VOL	DC output logic high voltage	-0.3		0.45	V

Table 2-17. I2S AC timing characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
f_{MCK}	Master clock frequency	0.768	-	49.152	MHz
f_{BCK}	Serial clock frequency	$32*f_S$	-	$64*f_S$	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	Output delay time. BCLK low to LRCK valid	-	-	13	ns
t_{V_DO}	Output delay time. BCLK low to SDOUT valid	-	-	13	ns
t_{S_DI}	DI setup time	16	-	-	ns
t_{H_DI}	DI hold time	16	-	-	ns

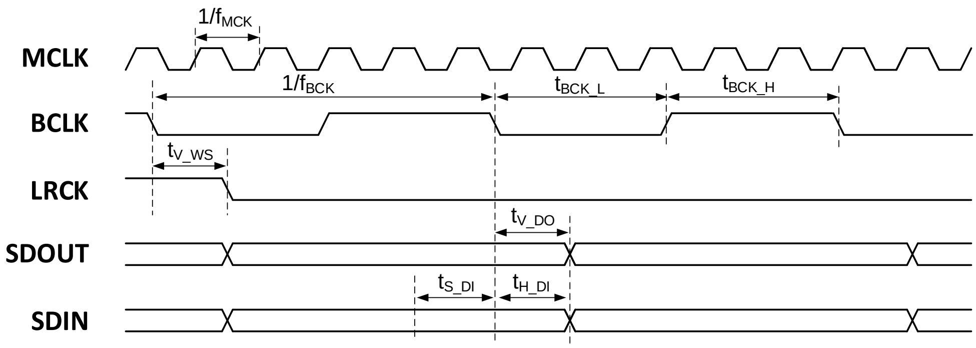

Figure 2-3. I2S master mode timing diagram

2.2.4.7 SIM DC Electrical Characteristics

Table 2-18. SIM DC electrical characteristics

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V

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Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V

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Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR4X

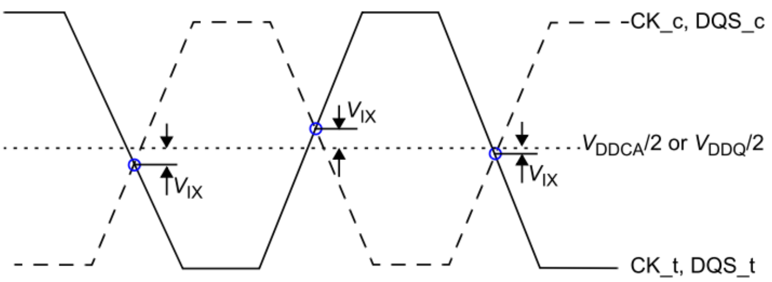

Figure 2-4. LPDDR4X VIX definition

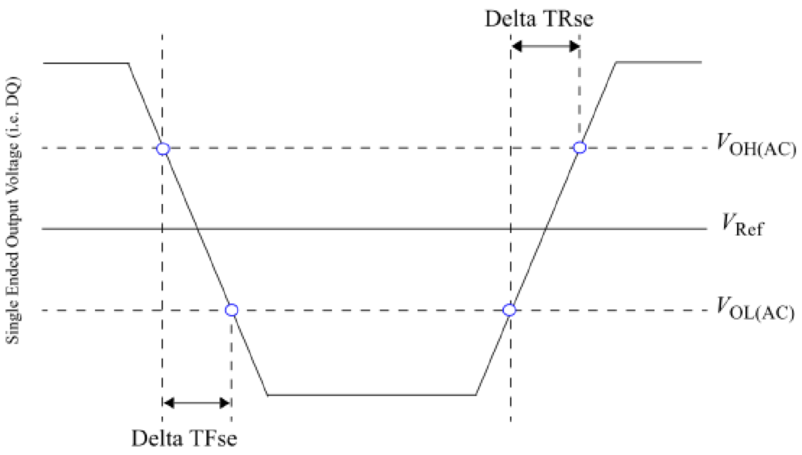

Figure 2-5. LPDDR4X single-ended output slew-rate definition

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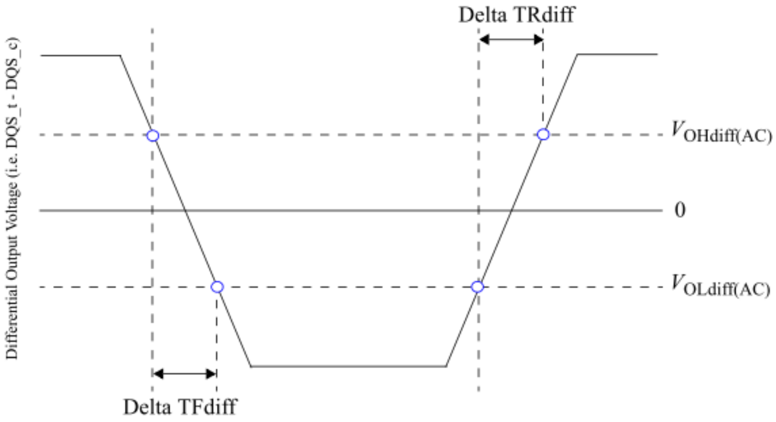

Figure 2-6. LPDDR4X differential output slew-rate definition

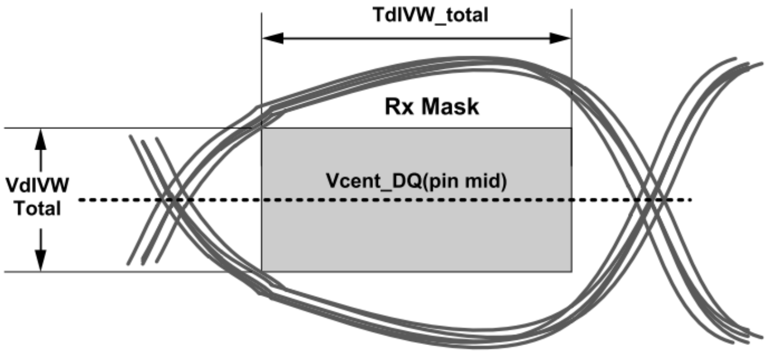

Figure 2-7. LPDDR4X Rx mask

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Table 2-19. LPDDR4X AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
Vix_DQS_ratio	DQS differential input crosspoint voltage ratio			20	%
Vix_CK_ratio	CK differential input crosspoint voltage ratio			25	%
SRQse (LPDDR4X)	Single-ended output slew rate	3		9	V/ns
SRQdiff (LPDDR4X)	Differential output slew rate	6		18	V/ns
VdIVW_total	Rx mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

2.2.5.2 SPI AC Timing Characteristics

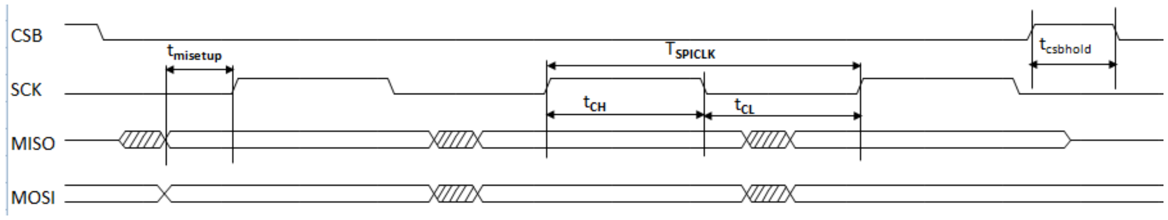

Figure 2-8. SPI timing diagram

Table 2-20. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	36.6	-	-	ns
SPI clock low time	t_{CL}	18.3	-	-	ns
SPI clock high time	t_{CH}	18.3	-	-	ns
SPI CSB hold time	$t_{csbhold}$	18.3	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

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2.2.5.3 I2S AC Timing Characteristics

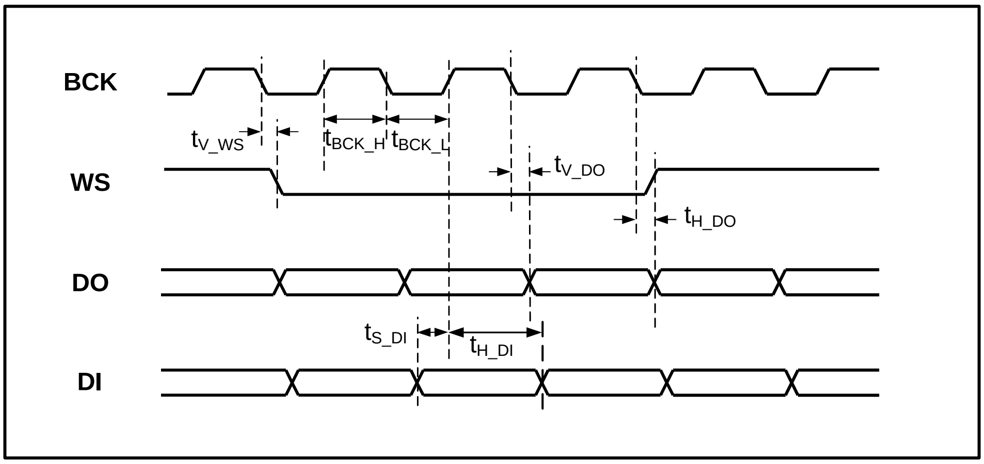

Figure 2-9. I2S master mode timing diagram

Table 2-21. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz
f_{BCK}	Serial clock frequency	$32*f_S$	-	$64*f_S$	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

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2.2.5.4 I2C AC Timing Characteristics

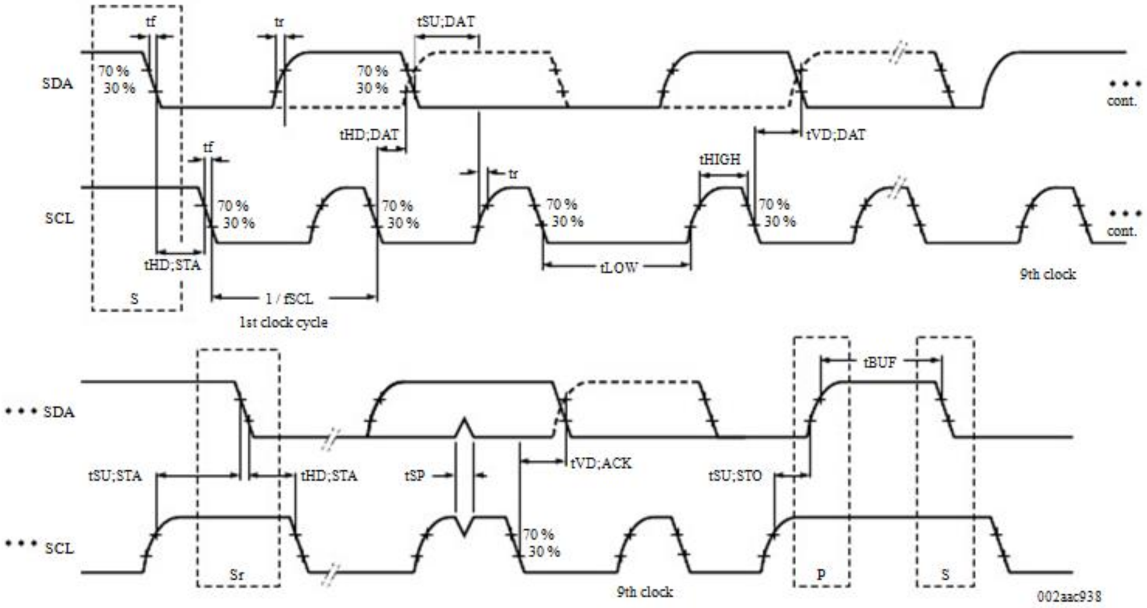

Figure 2-10. I2C timing diagram of standard mode (100 kHz) and fast mode (400 kHz)

Table 2-22. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

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2.2.5.5 MSDC AC Timing Characteristics

2.2.5.5.1 Default Speed Timing

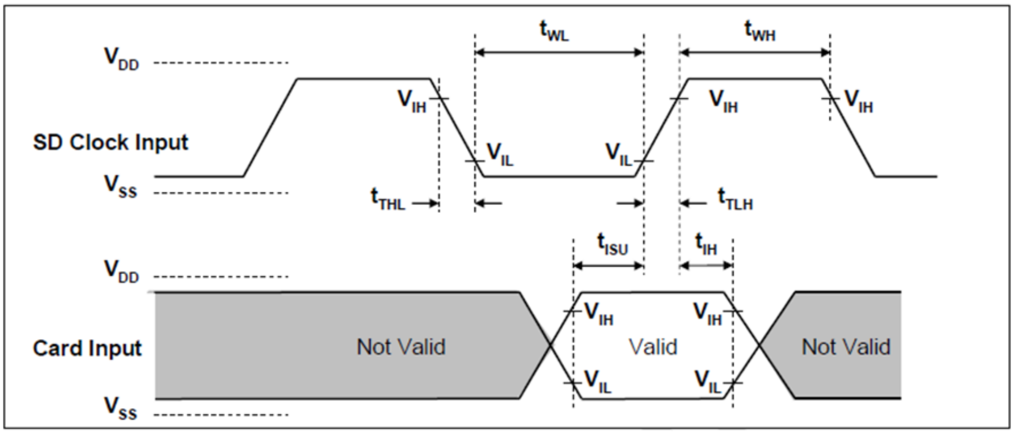

Figure 2-11. MSDC device input timing diagram of default speed

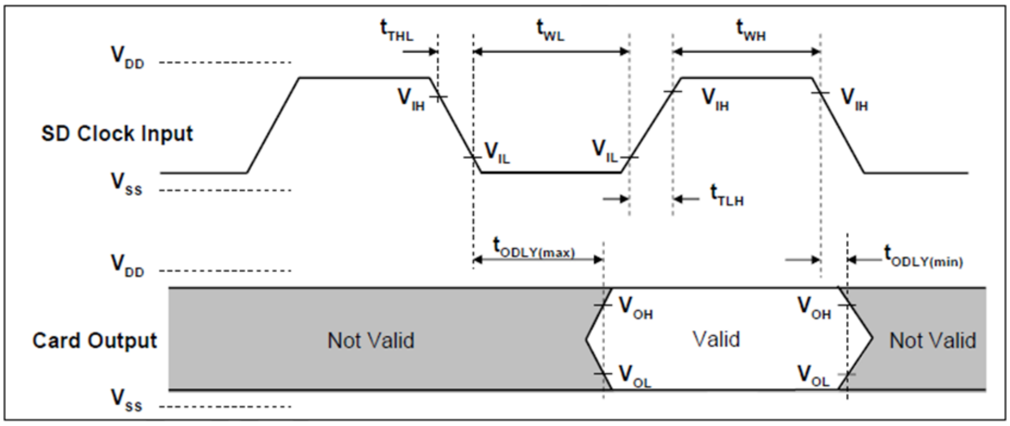

Figure 2-12. MSDC device output timing diagram of default speed

Table 2-23. MSDC device AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL}).)					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock frequency identification mode	f_{OD}	0/100	400	kHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD} ≤ 10 pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD} ≤ 10 pF (1 card)

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Parameter	Symbol	Min.	Max.	Unit	Remark
Input hold time	T_{IH}	5		ns	C_{CARD} ≤ 10 pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L ≤ 40 pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L ≤ 40 pF (1 card)

2.2.5.5.2 High Speed Timing

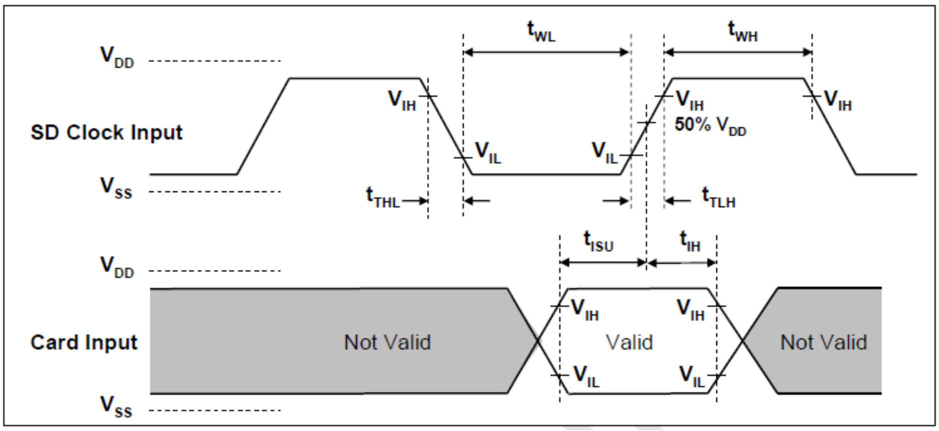

Figure 2-13. MSDC device input timing diagram of high speed

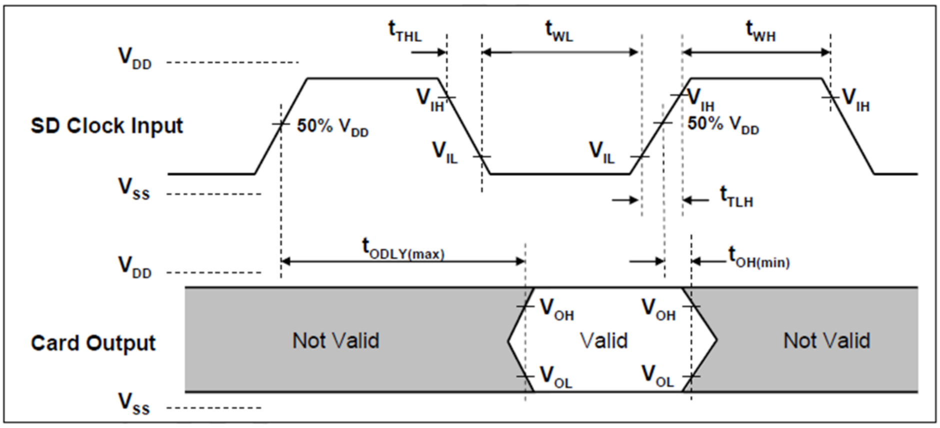

Figure 2-14. MSDC device output timing diagram of high speed

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Table 2-24. MSDC device AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL}).)					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD} ≤ 10 pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L ≥ 15 pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.5.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

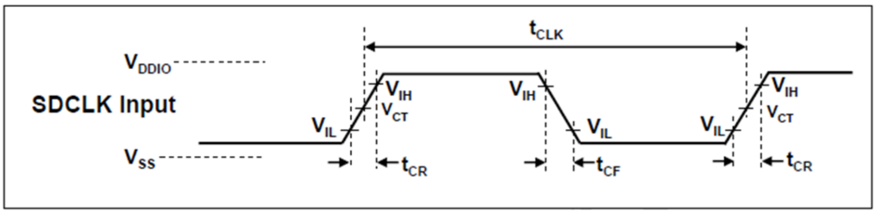

Figure 2-15. MSDC device clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

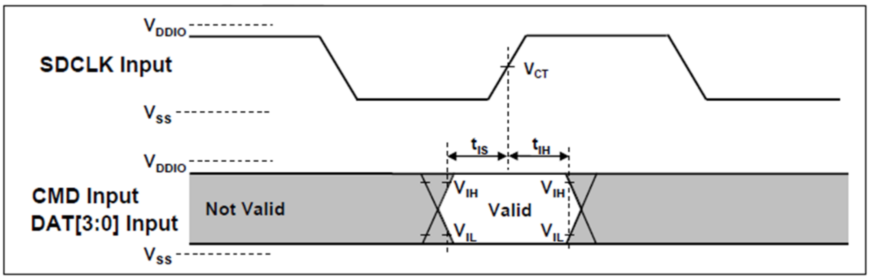

Figure 2-16. MSDC device input timing diagram of SDR50/SDR104 mode

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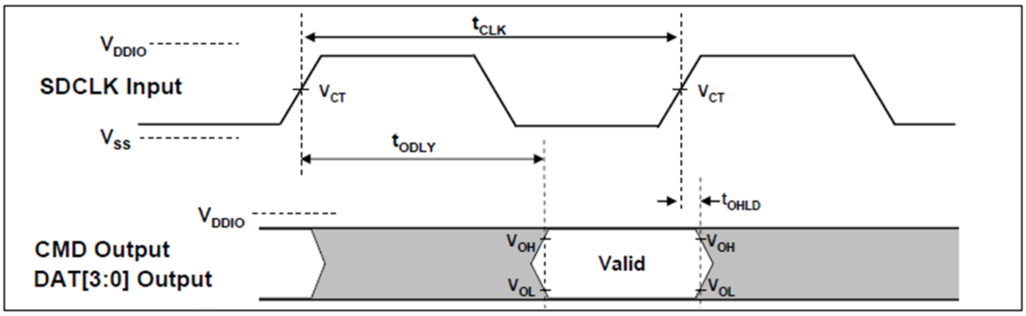

Figure 2-17. MSDC device output timing diagram of fixed data window (SDR12/SDR25/SDR50)

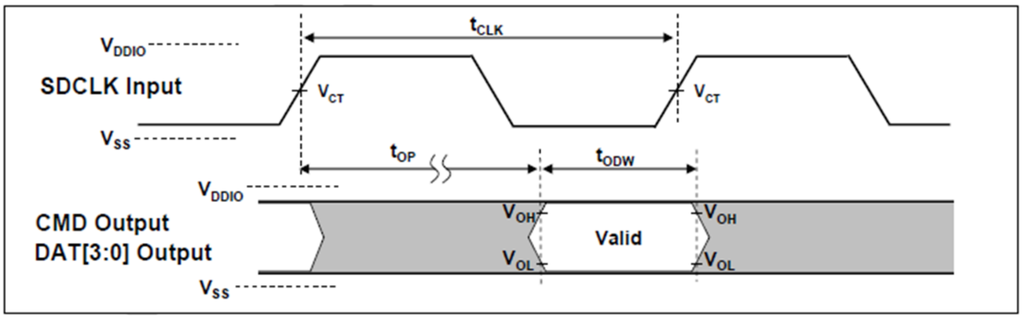

Figure 2-18. MSDC device output timing diagram of variable window (SDR104)

Table 2-25. MSDC device AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208 MHz (max.), between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96 ns (max.) at 208 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 2.00 ns (max.) at 100 MHz, C_{CARD} = 10 pF The absolute maximum value of t_{CR}, t_{CF} is 10 ns regardless of clock frequency.
Clock duty	30	70	%	
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD} = 10 pF, V_{CT} = 0.975V
t_{IH}	0.80		ns	C_{CARD} = 5 pF, V_{CT} = 0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD} = 10 pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5 pF, V_{CT} = 0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq$ 10.0 ns, C_L= 30 pF, using driver type B, for SDR50
t_{ODLY}		14	ns	$t_{CLK} \geq$ 20.0 ns, C_L= 40 pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L= 15 pF
Output CMD, DAT (SDR104)				

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Symbol	Min.	Max.	Unit	Remark
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1,550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW} = 2.88 ns at 208 MHz

2.2.5.5.4 DDR50 Speed Mode Timing

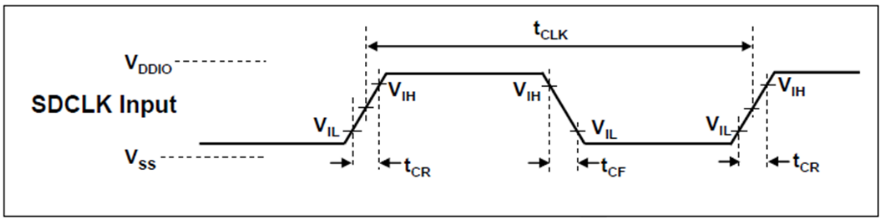

Figure 2-19. MSDC device clock timing diagram of DDR50 speed mode

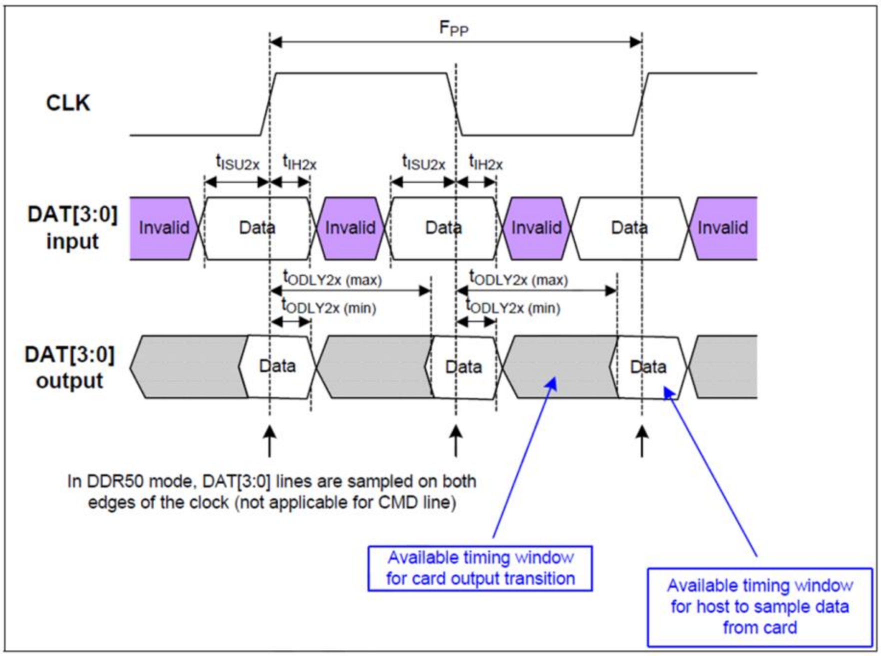

Figure 2-20. MSDC device input/output timing diagram of DDR50 speed mode

Table 2-26. MSDC device AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	$C_{CARD} \leq$ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} \leq$ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					

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Parameter	Symbol	Min.	Max.	Unit	Remark
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	$C_L \leq 30$ pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	$C_{CARD} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} \leq 10$ pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

2.2.5.5.5 HS200 Speed Timing

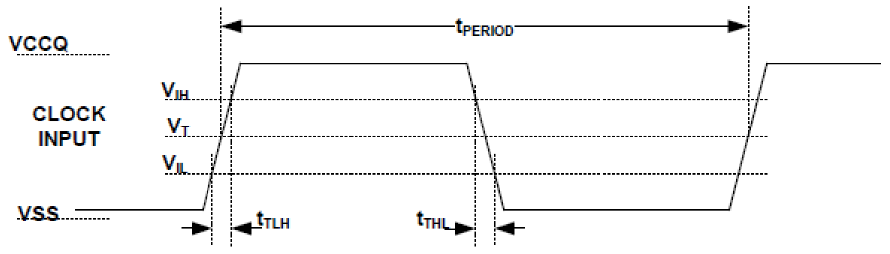
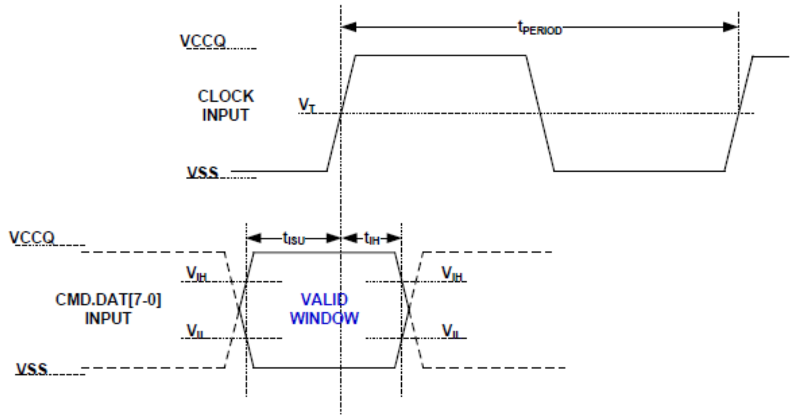


Figure 2-21. MSDC device clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-22. MSDC device input timing diagram of HS200

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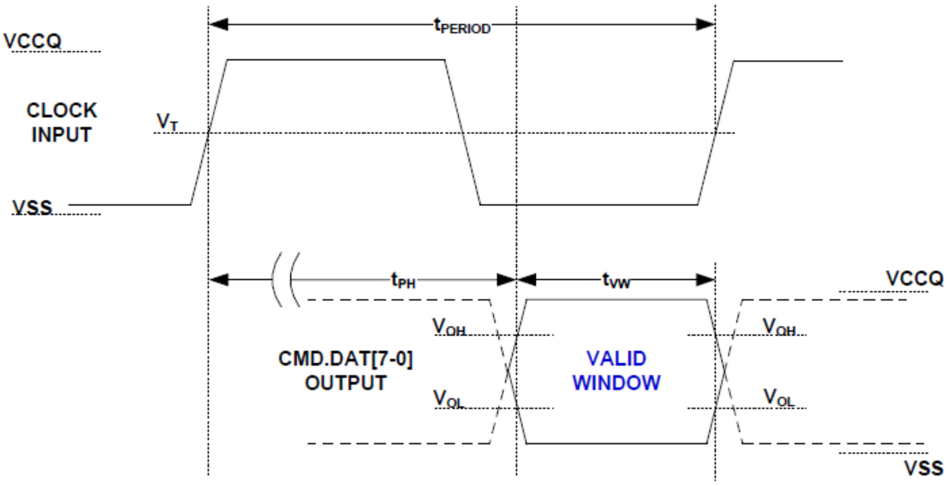

Figure 2-23. MSDC device output timing diagram of HS200

Table 2-27. MSDC device AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200 MHz (max.), between rising edge
t_{TLH}, t_{THL}	-	0.2*t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1 ns (max.) at 200 MHz, C_{DEVICE} = 6 pF The absolute maximum value of t_{TLH}, t_{THL} is 10 ns regardless of clock frequency.
Clock duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leq 6$ pF
t_{IH}	0.80		ns	$C_{DEVICE} \leq 6$ pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT = -20°C)	+1,550 (ΔT = 90°C)	ps	Delay varioation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system tuning procedure ΔT_{PH} is 2,600 ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW} = 2.88 ns at 208 MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI = 5 ns at 200 MHz.				

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2.2.5.5.6 HS400 Speed Timing

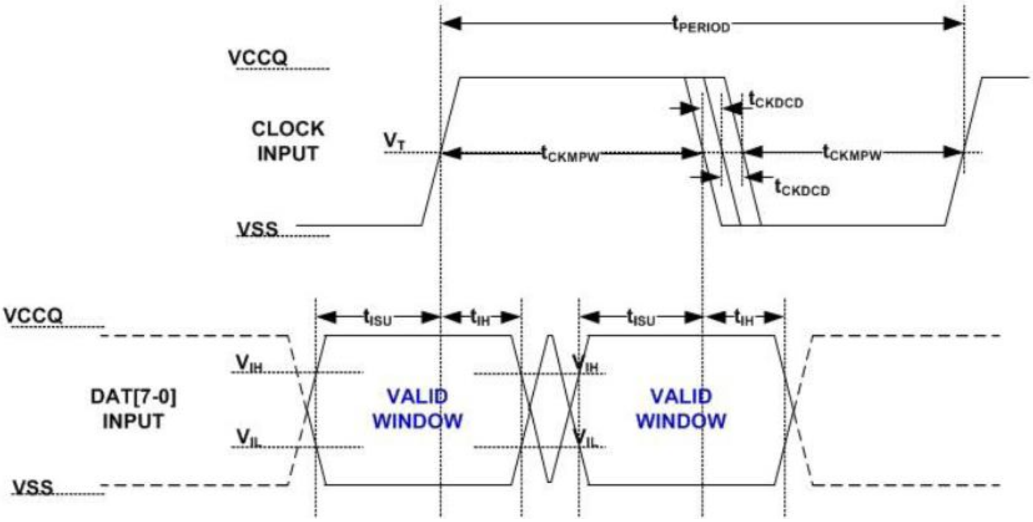

Figure 2-24. MSDC device input timing diagram of HS400

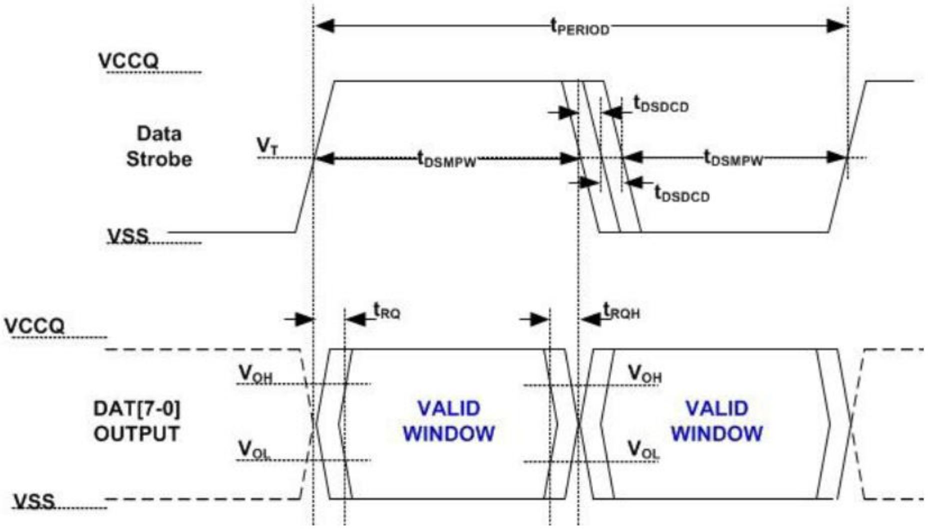

Figure 2-25. MSDC device output timing diagram of HS400

Table 2-28. MSDC device AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200 MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise

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Parameter	Symbol	Min.	Max.	Unit	Remark
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leq 6$ pF. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leq 6$ pF. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200 MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to data strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.6 SIM AC Timing Characteristics

Table 2-29. SIM AC timing parameters

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1,000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1,000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1,000	ns

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Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1,000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1,000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1,000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1,000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1,000	ns

2.2.6 Clock Squarer

2.2.6.1 Block Description

The clock squarer is designed to receive clock signal from pin “X26M_IN” and distribute it to the chip internally.

2.2.6.2 Functional Specifications

See the table below for the functional specifications of clock squarer of pin “X26M_IN”.

Table 2-30. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vin	Input signal amplitude	1,000	1,200	1,250	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN - 5		DcycIN + 5	%
	Maximum positive overshoot			1.3	V
	Minimum negative overshoot	-0.1			V

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-31. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI0 [1] PWRAP_SPI0_CSN	00: Use SPI pin for legacy JTAG, TDM pin for IO_JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG
[0] AUD_NLE_MOSI1	0: NA (default) 1: DP/DM output JTAG
[0] AUD_NLE_MOSI0	0: UFS booting 1: eMMC booting

2.3.2 Constant Tie Pins

Table 2-32. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

Refer to PMIC datasheet for detailed timing sequence.

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2.5 Package Information

2.5.1 Package Outlines

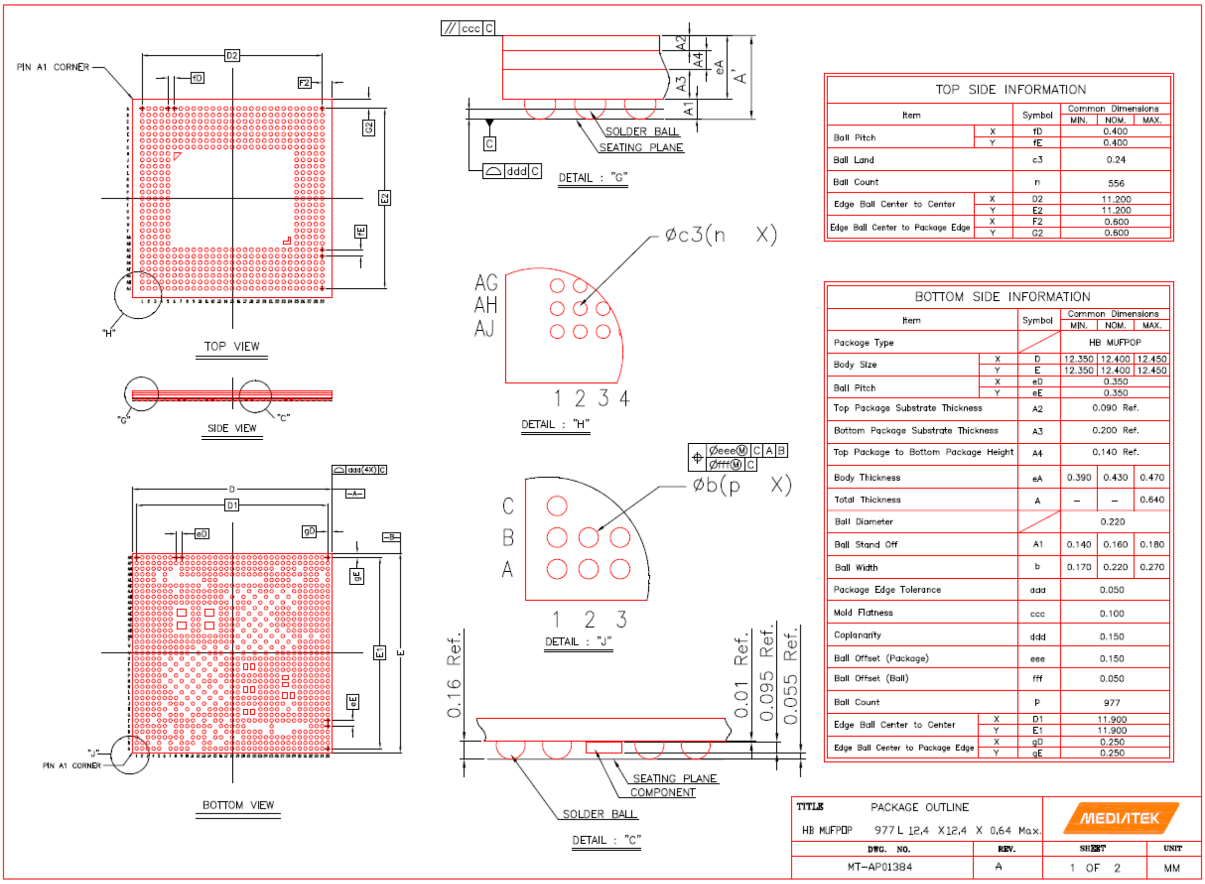

Figure 2-26. Outlines and dimensions of HBPOP 12.4 mm × 12.4 mm, 977-ball

2.5.2 Ordering Information

Order#	Marking	Temp. range	Package
MT6893Z/CZA	See 2.5.3.	-30~85°C	HBPOP

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2.5.3 Top Marking Definition

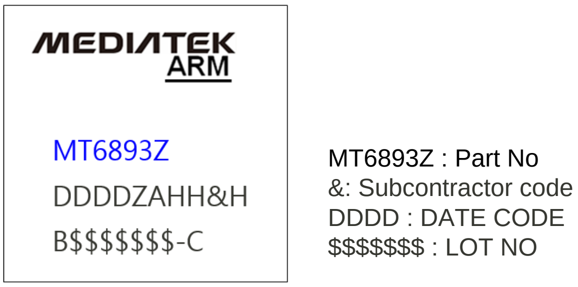

Figure 2-27. Top marking of MT6893Z

2.5.4 Thermal Operating Specifications

Table 2-33. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	21.57	°C/Watt	

2.5.5 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

2.5.6 MSL

The MSL of this chip is 3.

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